

# Compal Confidential

## DIS M/B Schematics Document

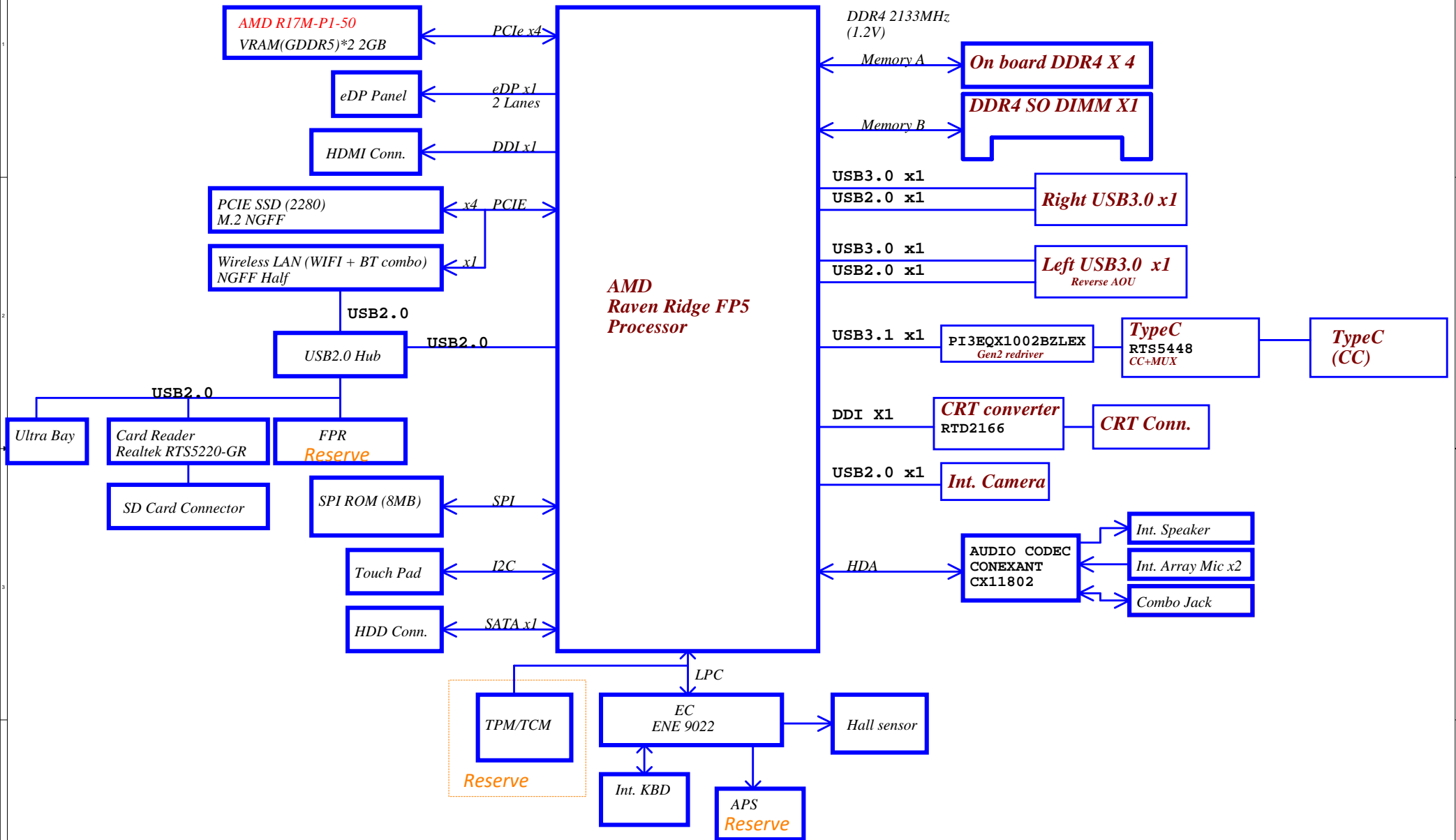
### AMD Raven Ridge FP5 APU with DDR4

### AMD R17M-M1-70

2017-04-17

LA-F484PR01

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Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_SOC	Core voltage for APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+0.8VALW	0.95V always on power rail	ON	ON	ON
+0.8VS	0.95V switched power rail	ON	OFF	OFF
+1.2V_DDR	1.2V power rail for APU and DDR	ON	ON	OFF
+2.5V_MEM	2.5V power rail for DDR	ON	ON	OFF
+0.6VS_VTT	0.6V switched power rail for DDR terminator	ON	OFF	OFF
+3VGS	3.3V switched power rail for VGA	ON	OFF	OFF
+1.8VGS	1.8V switched power rail for VGA	ON	OFF	OFF
+1.35VS_VRAM	1.35V switched power rail for VGA DDR	ON	OFF	OFF
+VDDCI	0.8V switched power rail for VGA	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON
+5VS	5V switched power rail	ON	OFF	OFF
+RTC_APU	RTC power	ON	ON	ON

SMBUS Control Table

	SOURCE	VGA	BATT	EC	SODIMM	WLAN	APU
EC_SMB_CK1 EC_SMB_DA1	9022 +3VALW	X	V +3VALW	V +3VALW	X	X	X
APU_SCLK0 APU_SDATA0	APU +3VS	X	X	X	V +3VS	X	X
EC_SMB_CK2 EC_SMB_DA2	9022 +3VS	X	X	V +3VALW	X	X	V +1.8VS (+3VS)

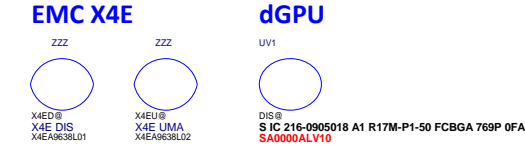
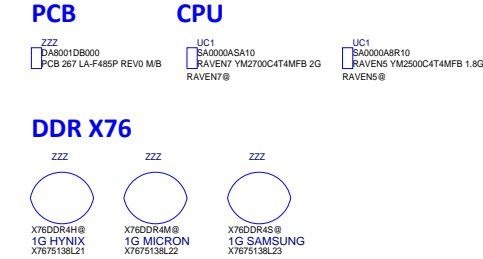
EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	GPU	0x41/0x41	
Charger	0001 0010 b	12H	APS	3Dh/3Ch	
			VGA Converter	0x64/0x65	

USB OC MAPPING

OC#	USB Port	
0	USB20_0_port2	
1	USB20_1_port0	
2	USB HUB	
3		

APU SM Bus address			
SM Bus 0	Device	Address	HEX
	DDR DIMM1	1010 001Xb	A2H
APU I2C Bus address			
I2C 3	Device	Address	
	Touch Pad (Synaptics)	S2C	
	Touch Pad (Elan)	0X15	

STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF



Card Reader X76



GPP Port Table

Port	Device
GPP0	
GPP1	
GPP2	SSD (PCIE)
GPP3	
GPP4	LAN (PCIE)
GPP5	WLAN (PCIE)
GPP6	HDD (SATA)
GPP7	

DisplayPort Table

Port	Device
0	eDP
1	HDMI
3	DisplayPort -> CRT
2	

USB3.0 Port Table

Port	Device
0	
1	Type C Right
2	USB3.0 Left
3	USB3.0 Right
4	

USB2.0 Port Table

Port	Device
0	Camera
1	Type C Right
2	USB3.0 Left
3	USB3.0 Right
4	
5	USB Hub
5-1	Card Reader
5-2	BT
5-3	Ultra Bay
5-4	FP

BOM Structure Table

BOM Structure	Item
UMA@	For UMA
DIS@	For DIS
VGAEMIE@	EMI VGA pop component
EMI@	EMI pop component
@EMI@	EMI Unpop component
ESD@	ESD pop component
@ESD@	ESD Unpop component
VGAESD@	ESD VGA pop component
RF@	RF pop component
@RF@	RF Unpop component
@	Unpop
VGA@	VGA component
CMOS@	Camera component
FP@	Finger Print Component
KBL@	KeyBoard Backlight component
HDT@	For HDT Debug used
TPM@	TPM Component
TCM@	TCM Component
NOTPM@	No TPM/TCM Component
AOU@	AOU Component
NONAOU@	NONAOU Component
APS@	APS Component
NONAPS@	No APS Component
TYPEC@	TYPEC 5457 component
NONTYPEC@	No TYPEC 5457 component
BATT2@	2nd BATT USB Component
NONBATT2@	Non 2nd BATT USB Component
8M@	BIOS 8M
16M@	BIOS 16M
X4ED@	EMC component for DIS
X4EU@	EMC component for UMA
STE@	Stereo SPK
MONO@	Mono SPK
ME@	ME part
X76RT@	Card Reader Realtek
X76GL@	Card Reader GENESYS
X76DDR4H@	Onboard RAM HYNIX
X76DDR4M@	Onboard RAM MICRON
X76DDR4S@	Onboard RAM SAMSUNG
X76@	X76 part
H2G@	For HYNIX 2G VRAM
S2G@	For SAMSUNG 2G VRAM
M2G@	For MICRON 2G VRAM
RAVEN7@	RAVEN7 CPU
RAVEN5@	RAVEN5 CPU

LA-F484P Power Sequence

Boot

Shut  
Down

EC Pin 110 Input

EC Pin 112 Output

AC Plug

EC Pin 114 Input

EC Pin 100 Output

EC Pin 122 Output

EC Pin 123 Input

EC Pin 6 Input

EC Pin 95 Output

EC Pin 116 Output

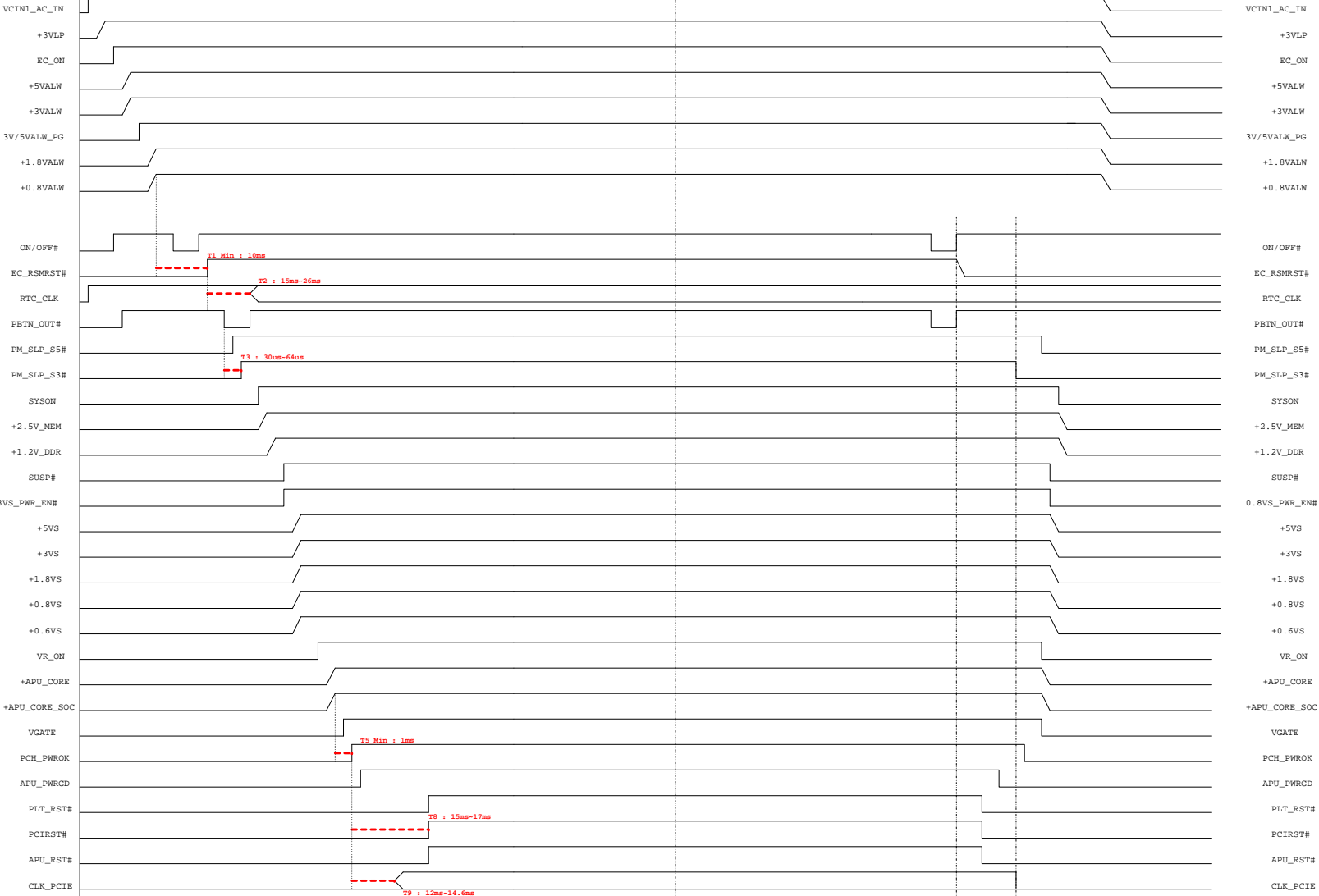
EC Pin 99 Output

EC Pin 121 Output

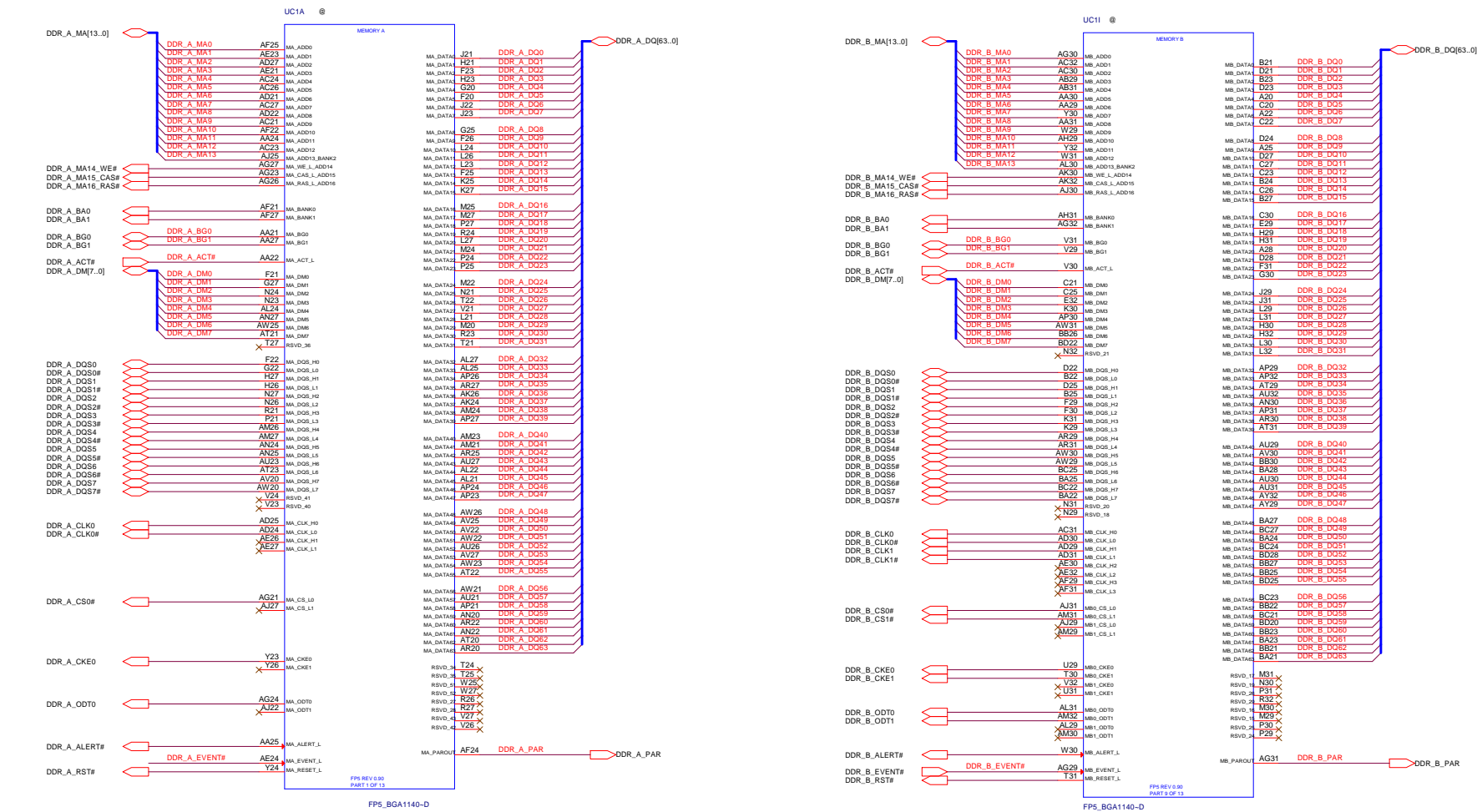
EC Pin 36 Input

EC Pin 32 Output

EC Pin 13 Input



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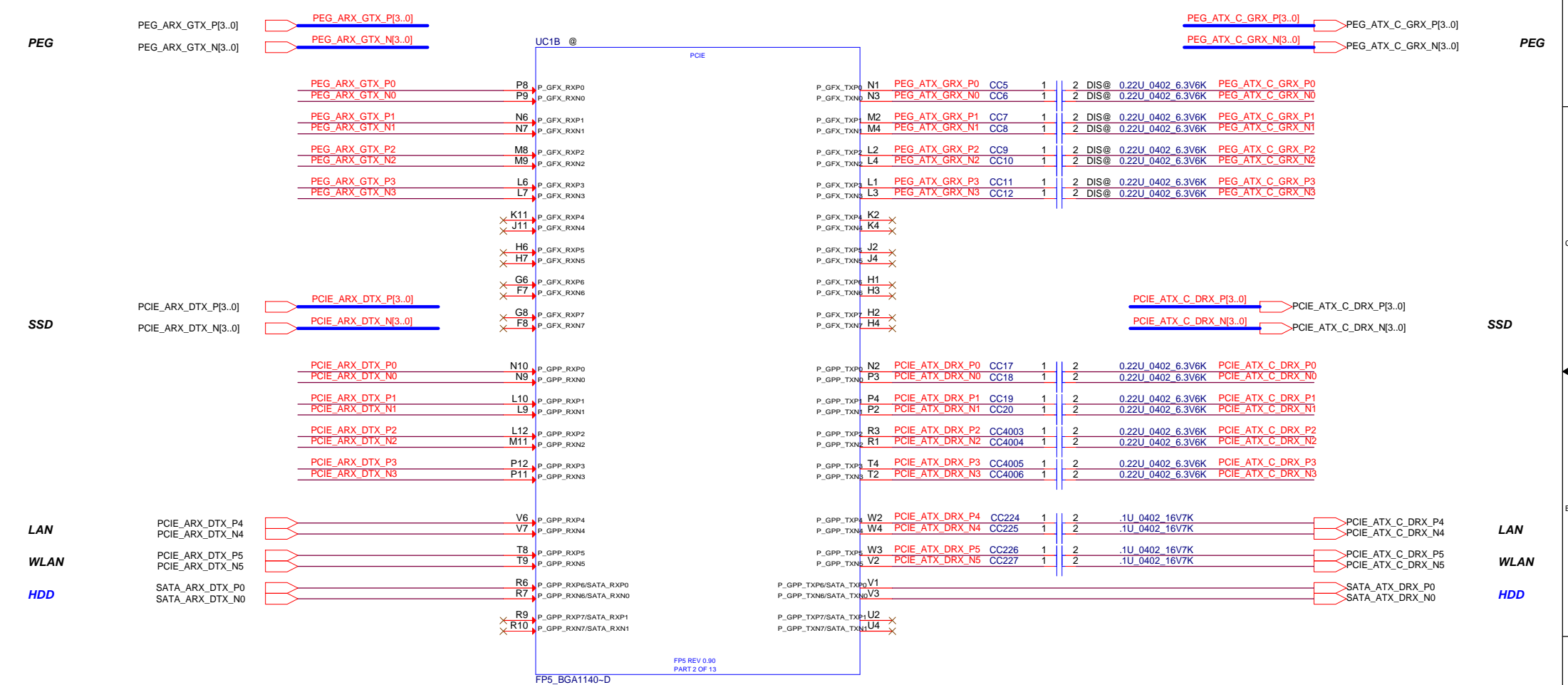
EVENT# pull high



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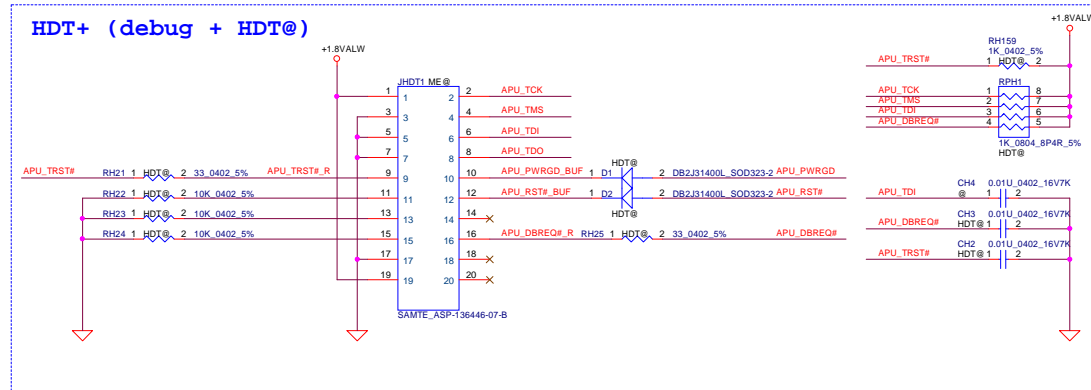
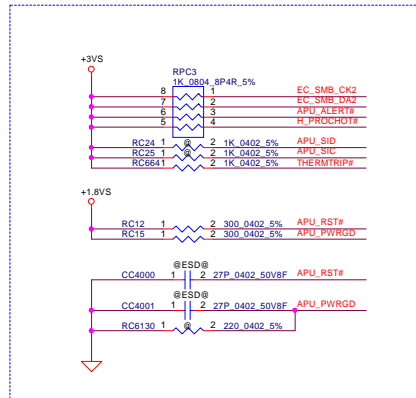
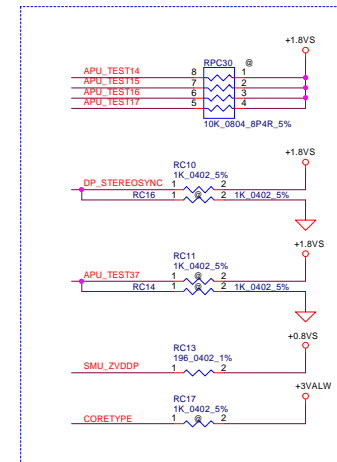
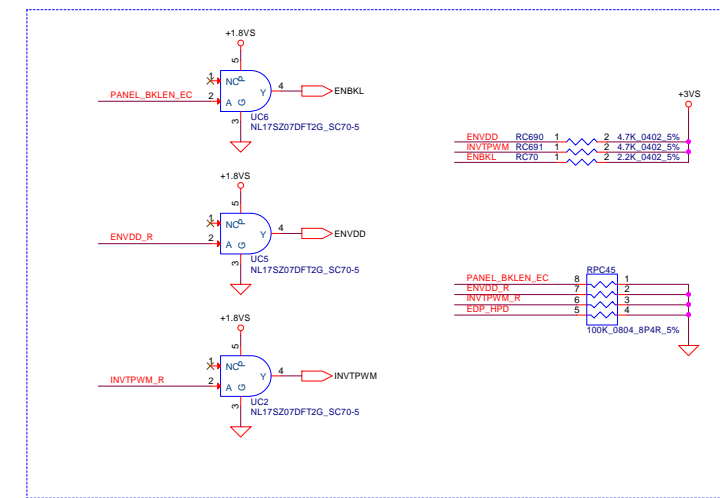
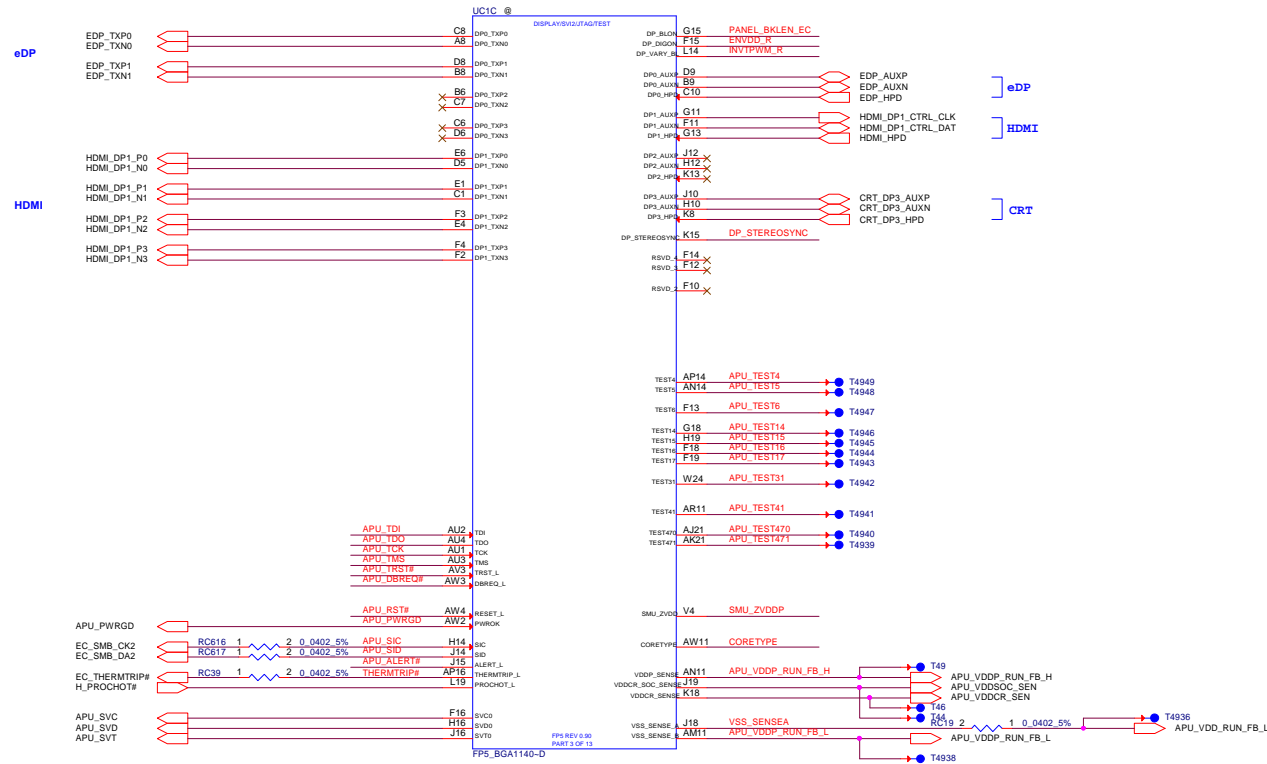
Main Func = CPU



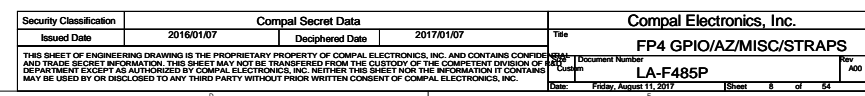
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Size Custom	Document Number	Rev		0.1	
LA-F485P		Date:		Friday, August 11, 2017	
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Main Func = CPU

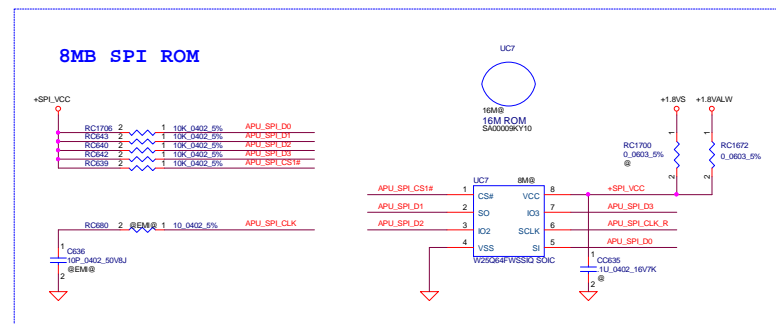
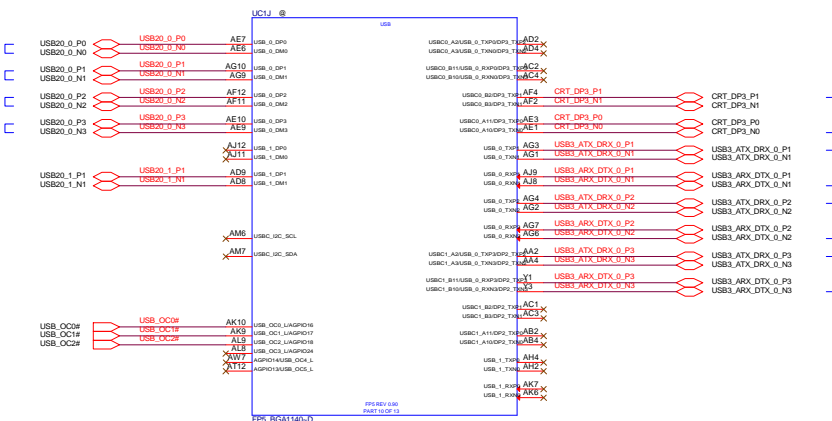
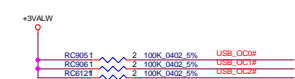
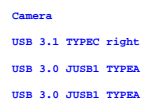
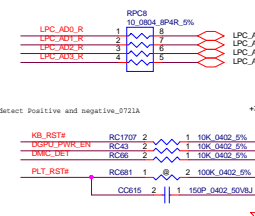
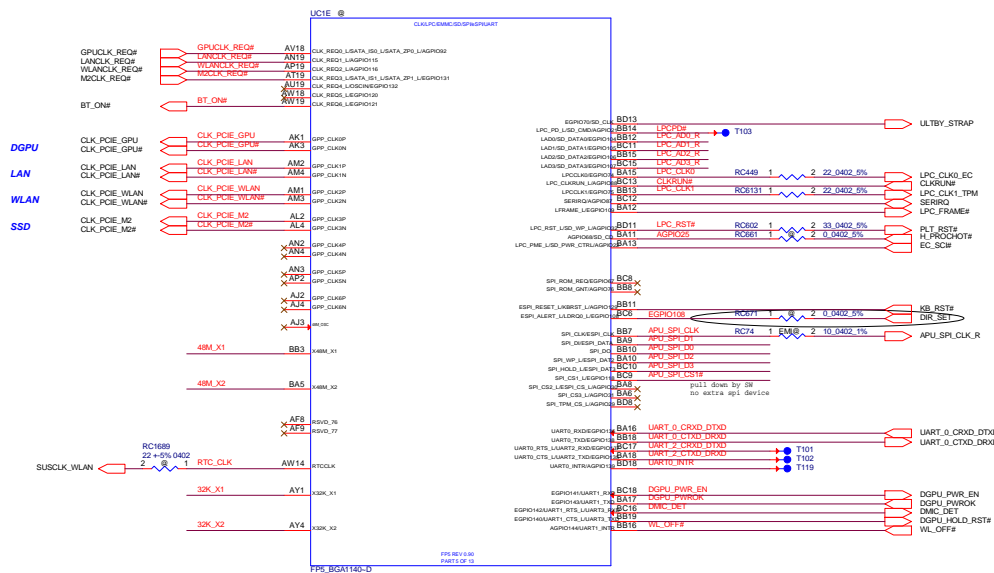
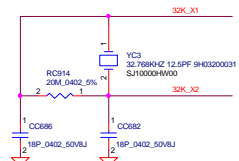
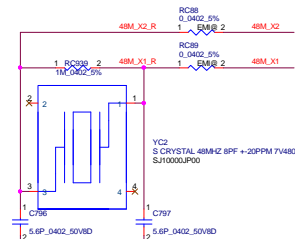
```
DP0: eDP
DP1: HDMI
DP2: N/A
DP3: DisplayPort -> CRT
```



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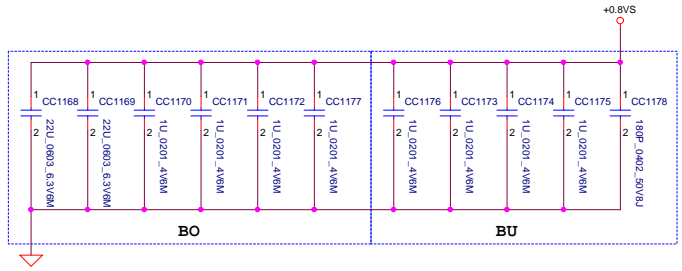
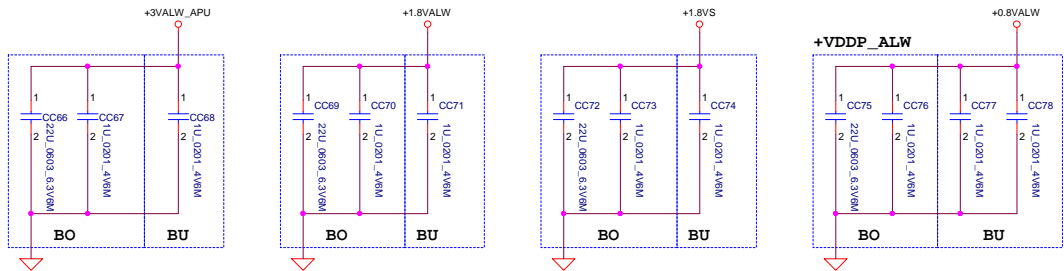
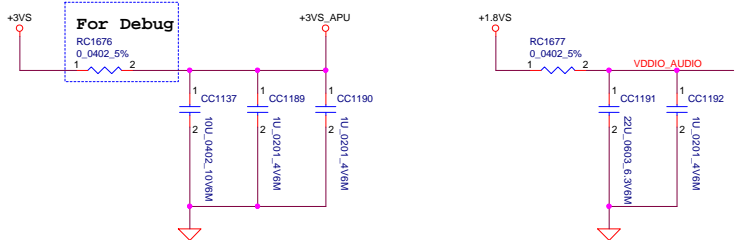
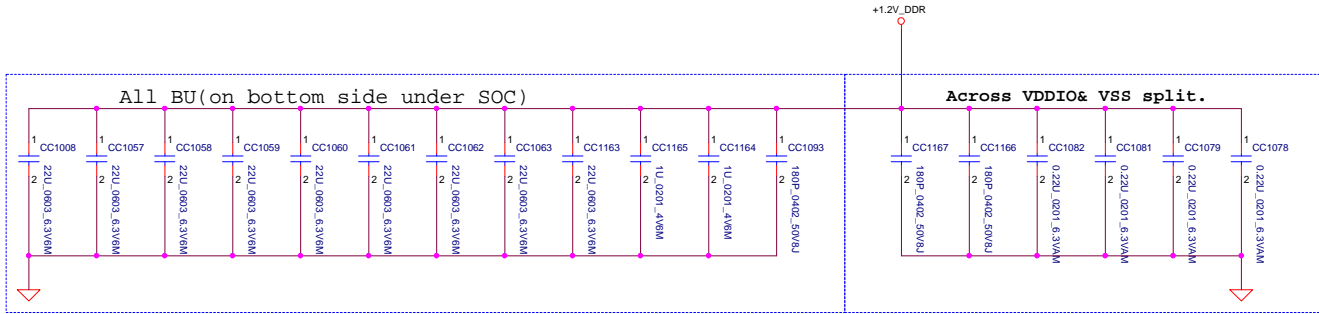




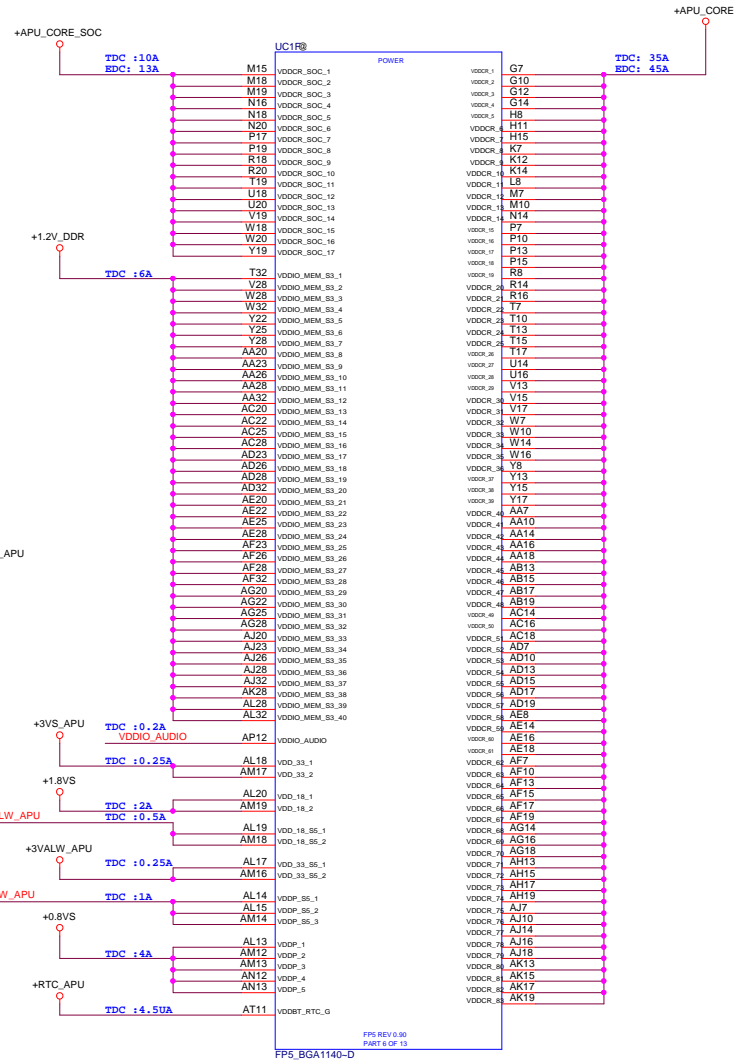
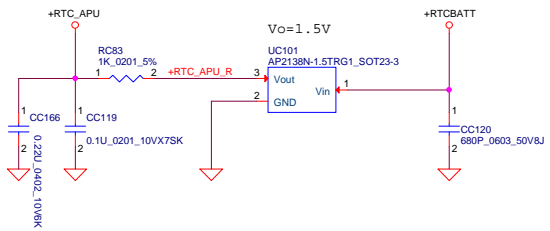


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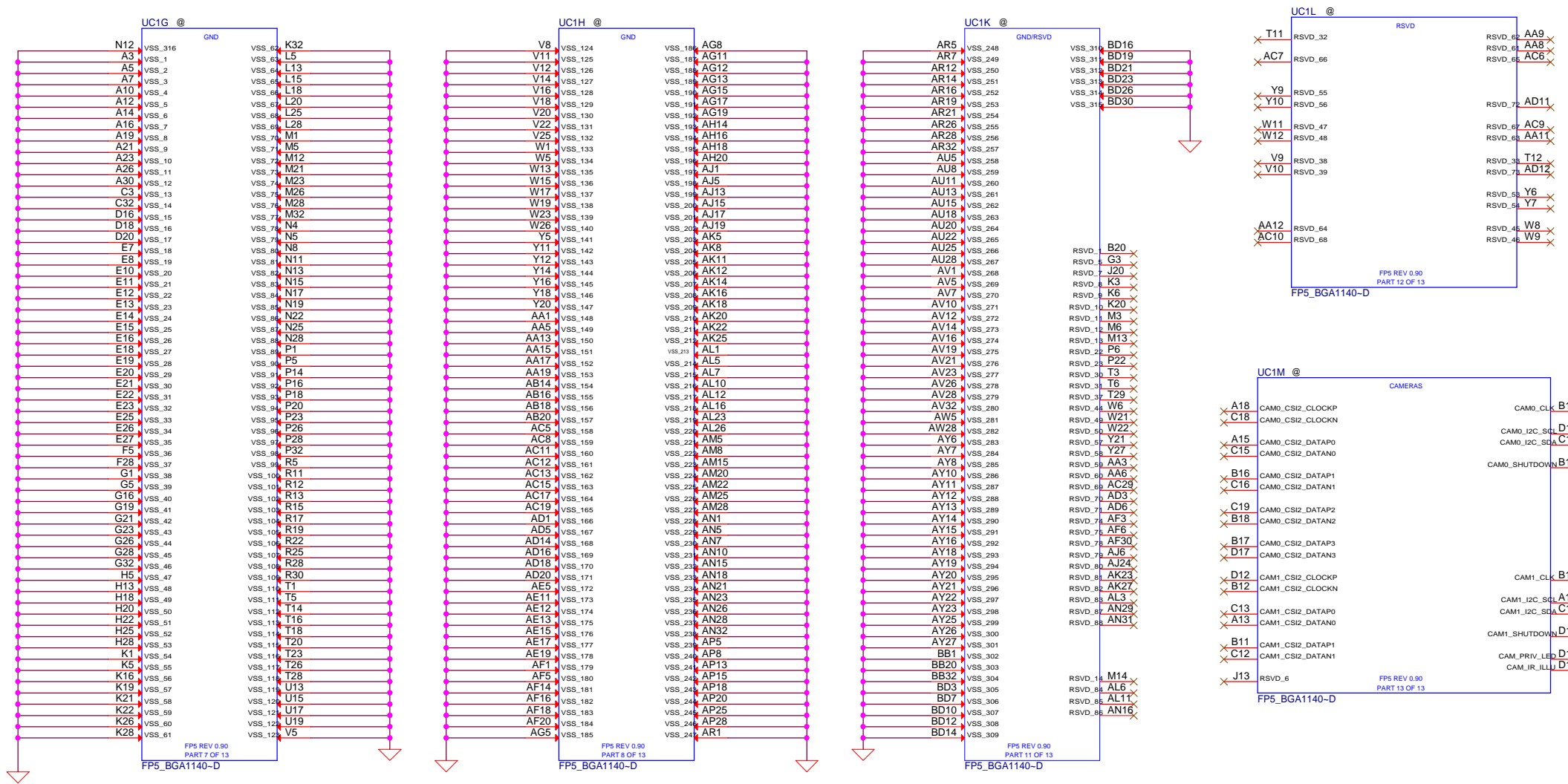
Main Func = CPU



RTC OF APU



Main Func = CPU



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# Memory Down

5/10A 55597\_FP5 Processor Motherboard Design Guide P.86

1.2V\_DDR  
+0.6VS\_VTT  
+0.6V\_DDR\_VREFCA

Memory Side

2/17 55346\_FT4 Processor Motherboard Design Guide P.276  
ZQ Max Length : 1968 mil

3/9 Add reserve resistor for DDP DDR

3/1 For +2.5V\_MEM (Ref CX50 LA-E521PR02\_1101)

DRAM DOWN DECOUPLING

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DDR4 CHA SO-DIMM  
LA-F48SP  
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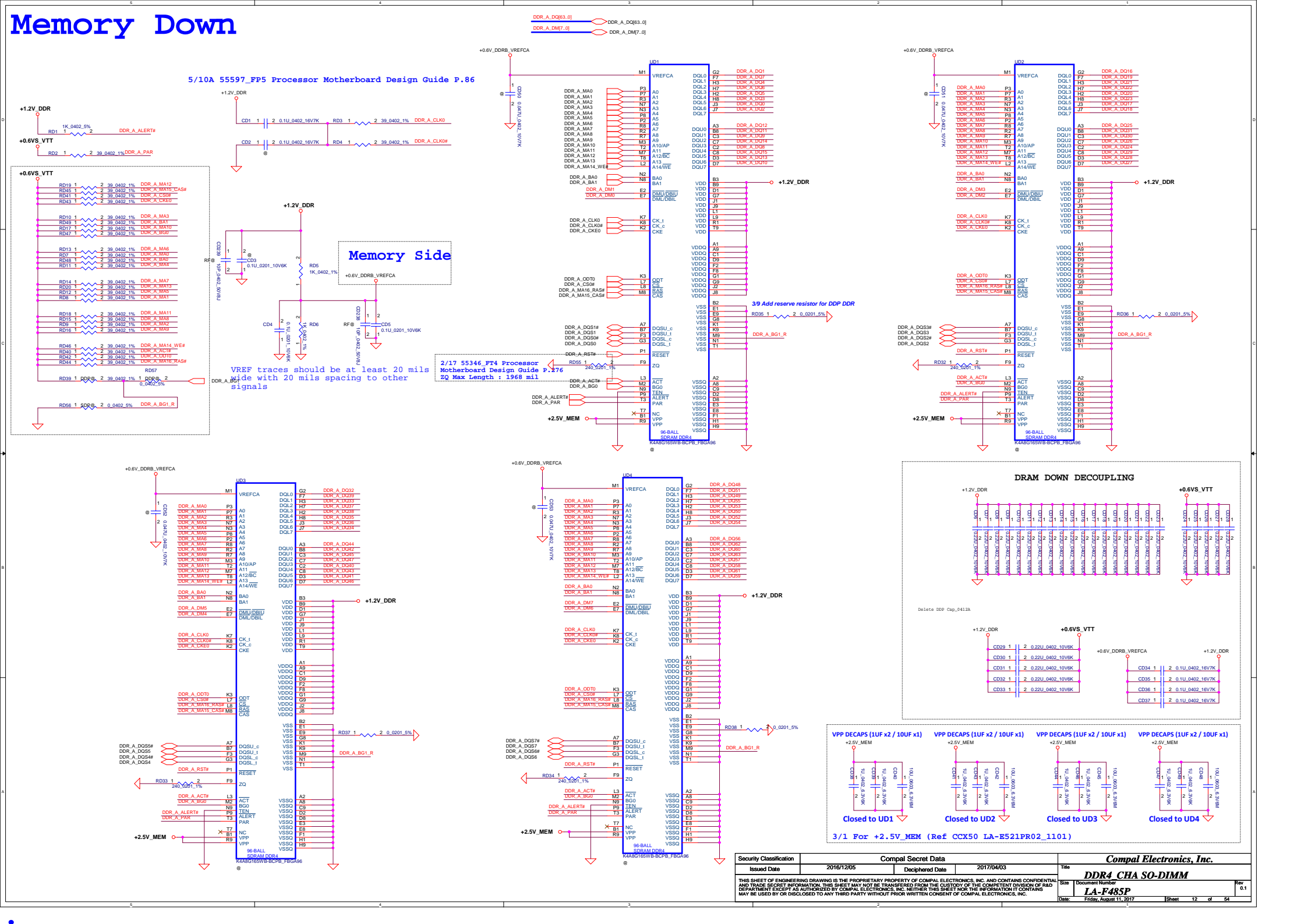
3/1 For +2.5V\_MEM (Ref CX50 LA-E521PR02\_1101)

DRAM DOWN DECOUPLING

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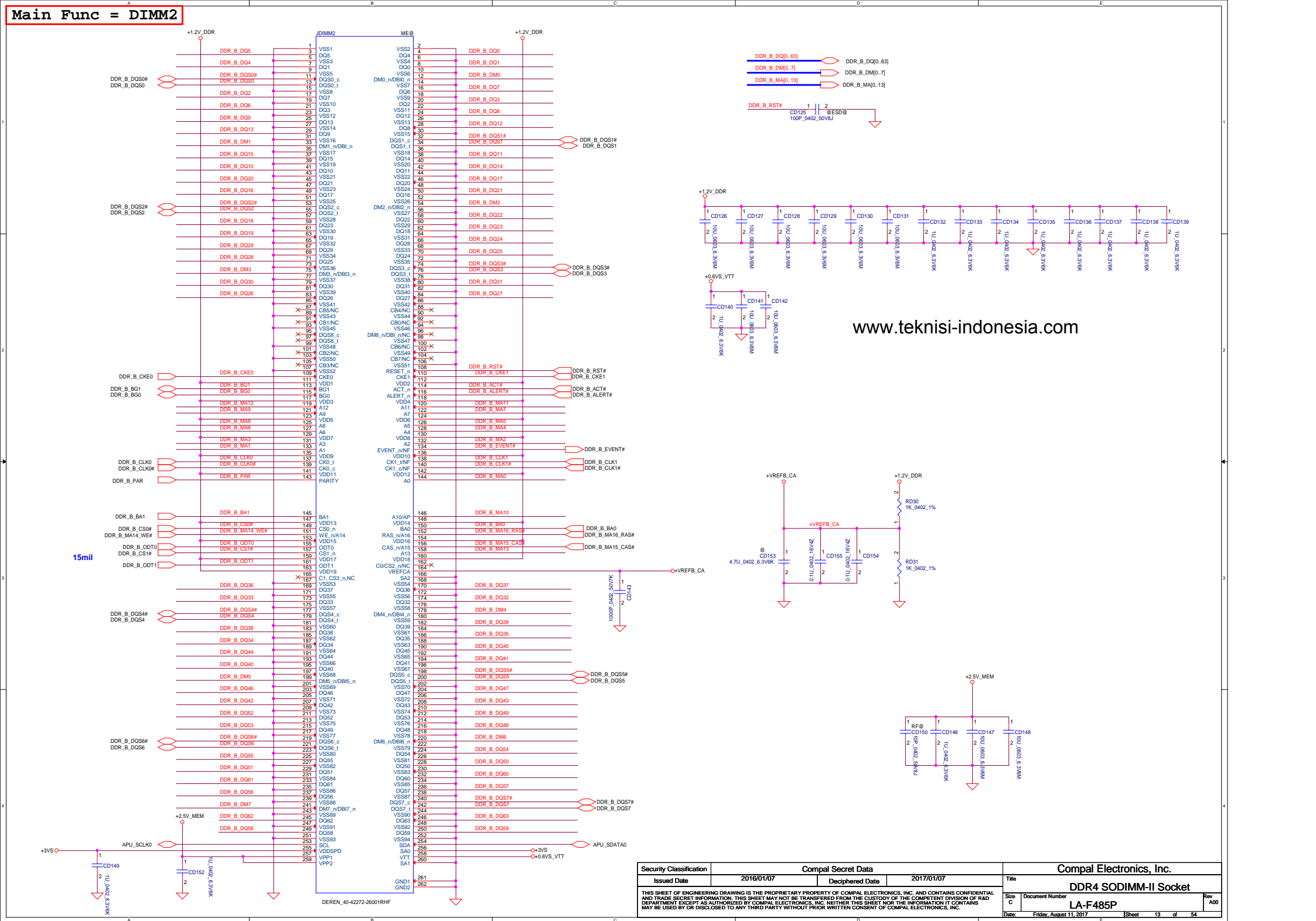
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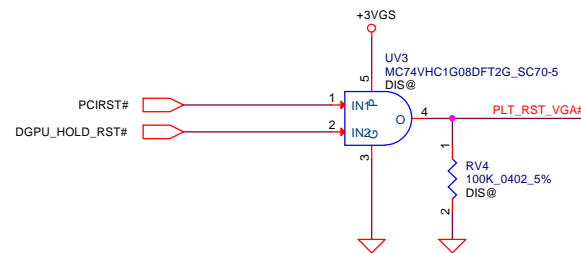
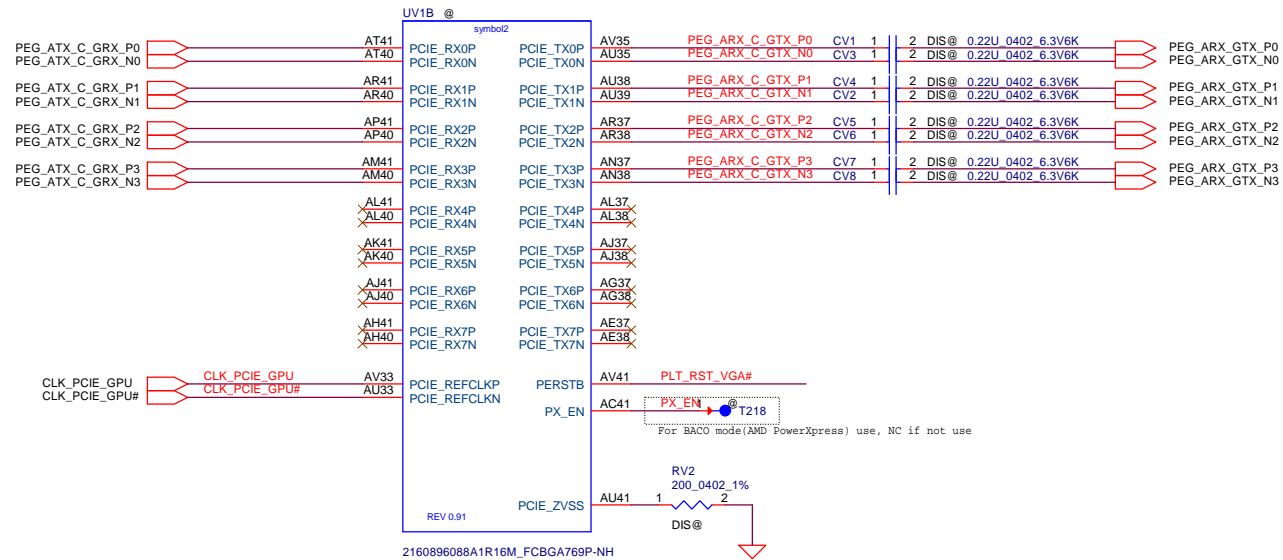
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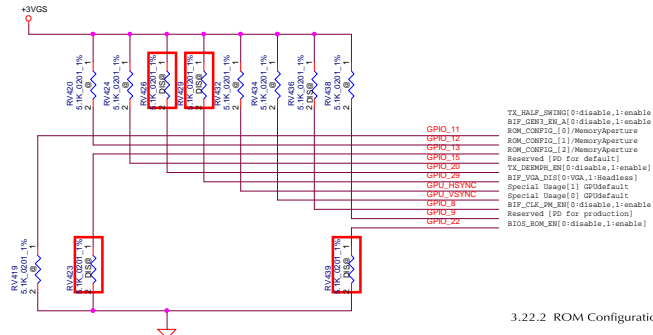
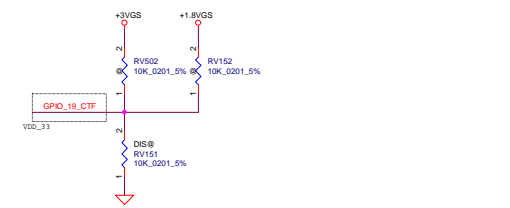
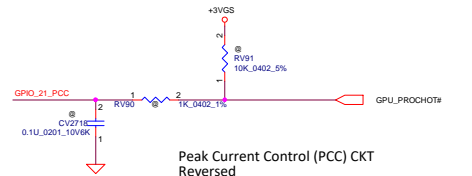
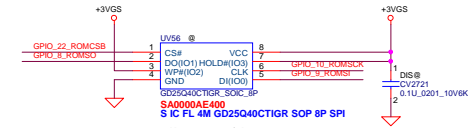
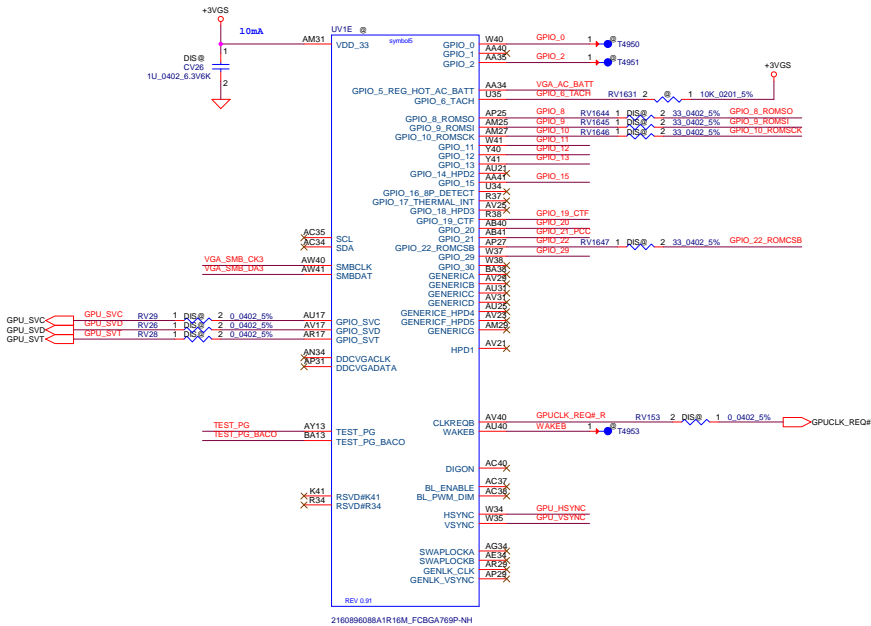
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Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
8 GB	011
16 GB	100
1 GB	101
2 GB	110
4 GB	111

For designs that have a dedicated ROM device for the GPU video BIOS:

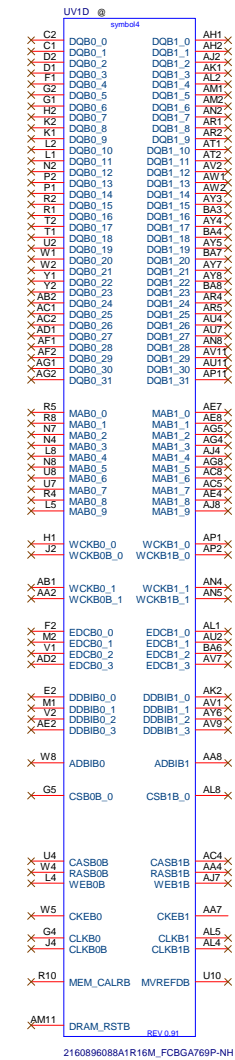
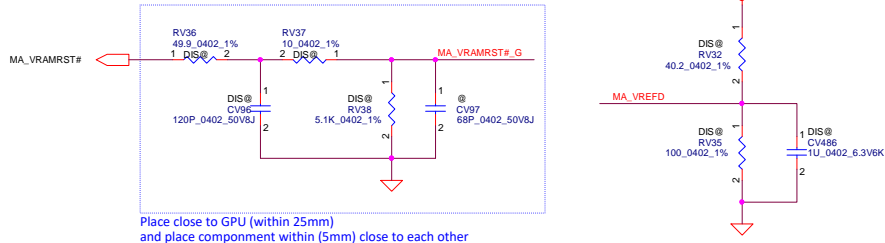
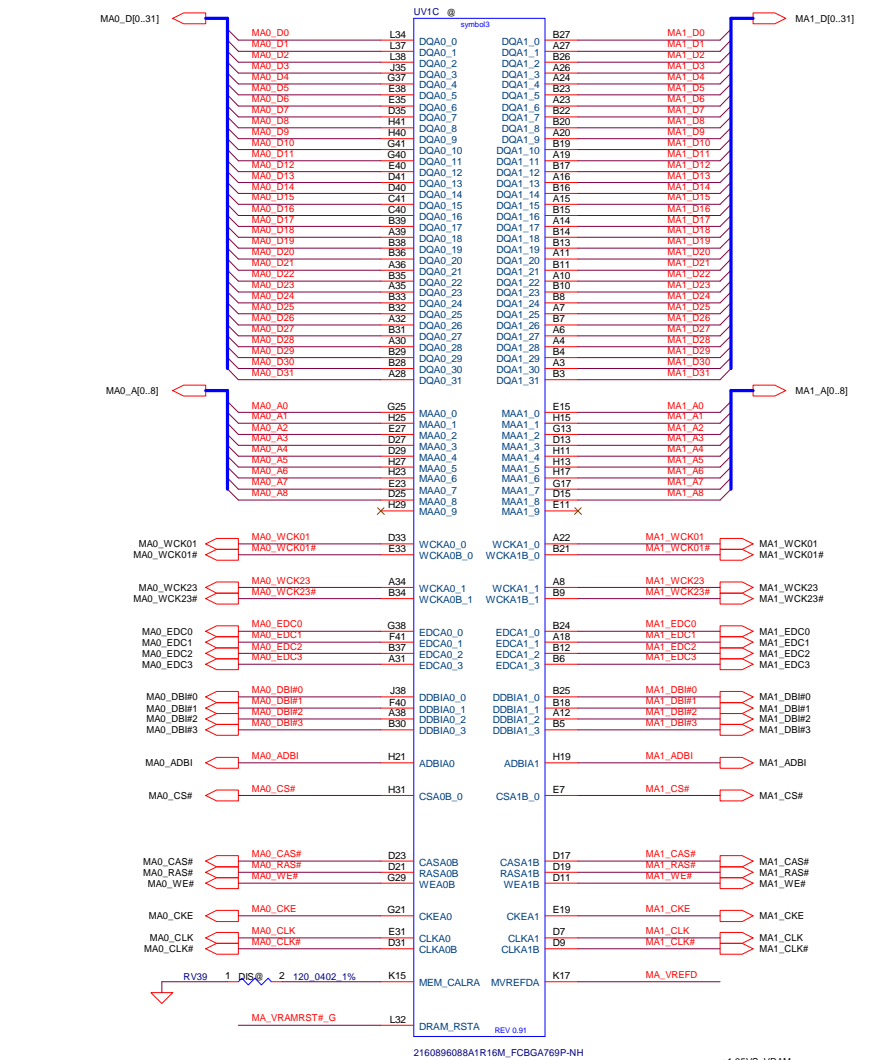
- Use the GPU default strap on GPIO\_22\_ROMCSB (i.e., 1).
- Use the GPU default straps on GPIO\_13, GPIO\_12, and GPIO\_11 (i.e., 101).

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				Date:	Friday, August 11, 2017	Sheet 15 of 54

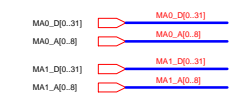




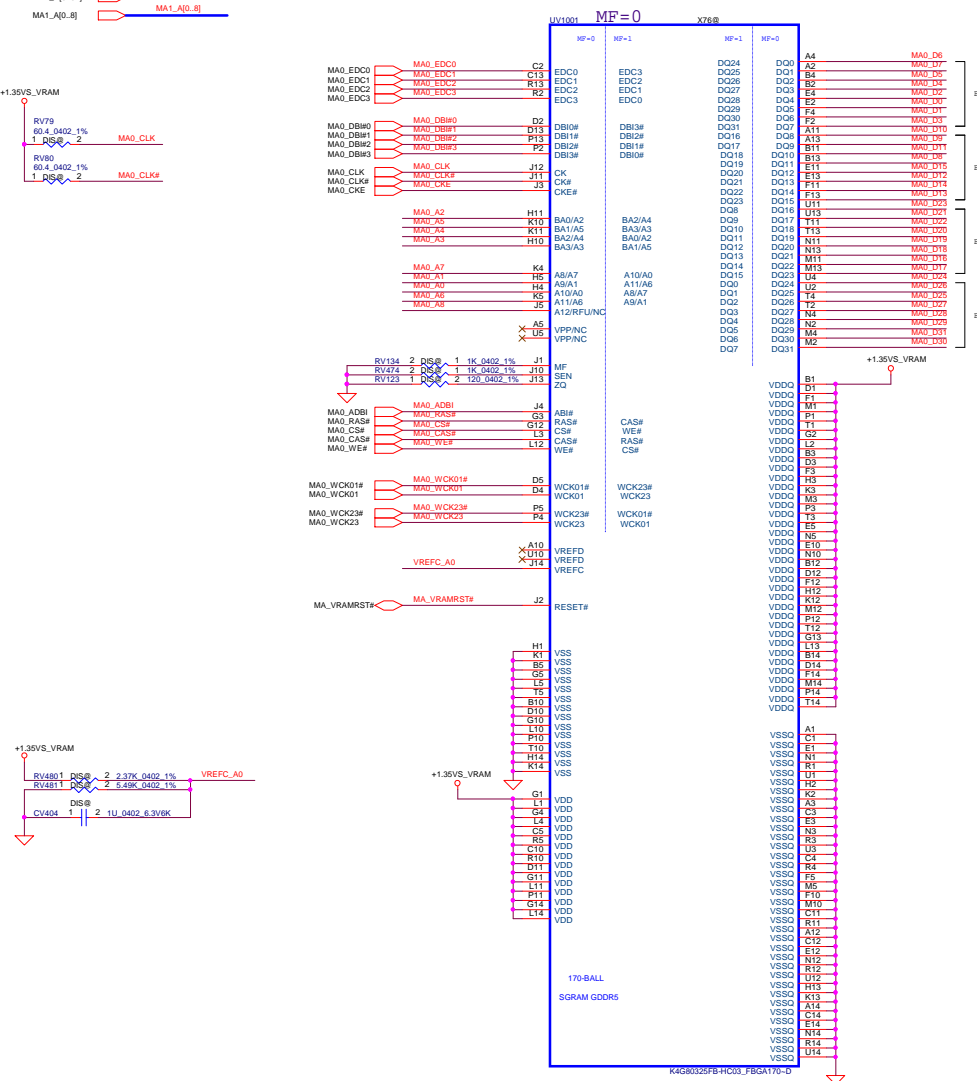




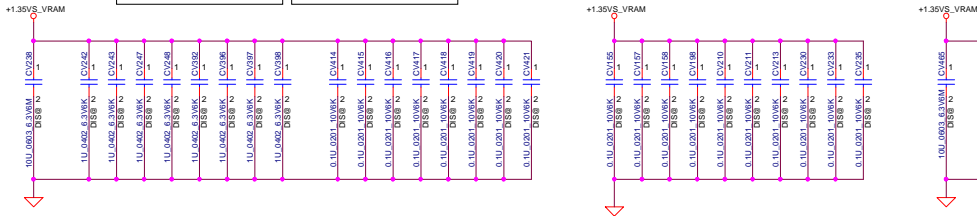
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Issued Date	2017/04/18	Deciphered Date	2019/04/18	Title	
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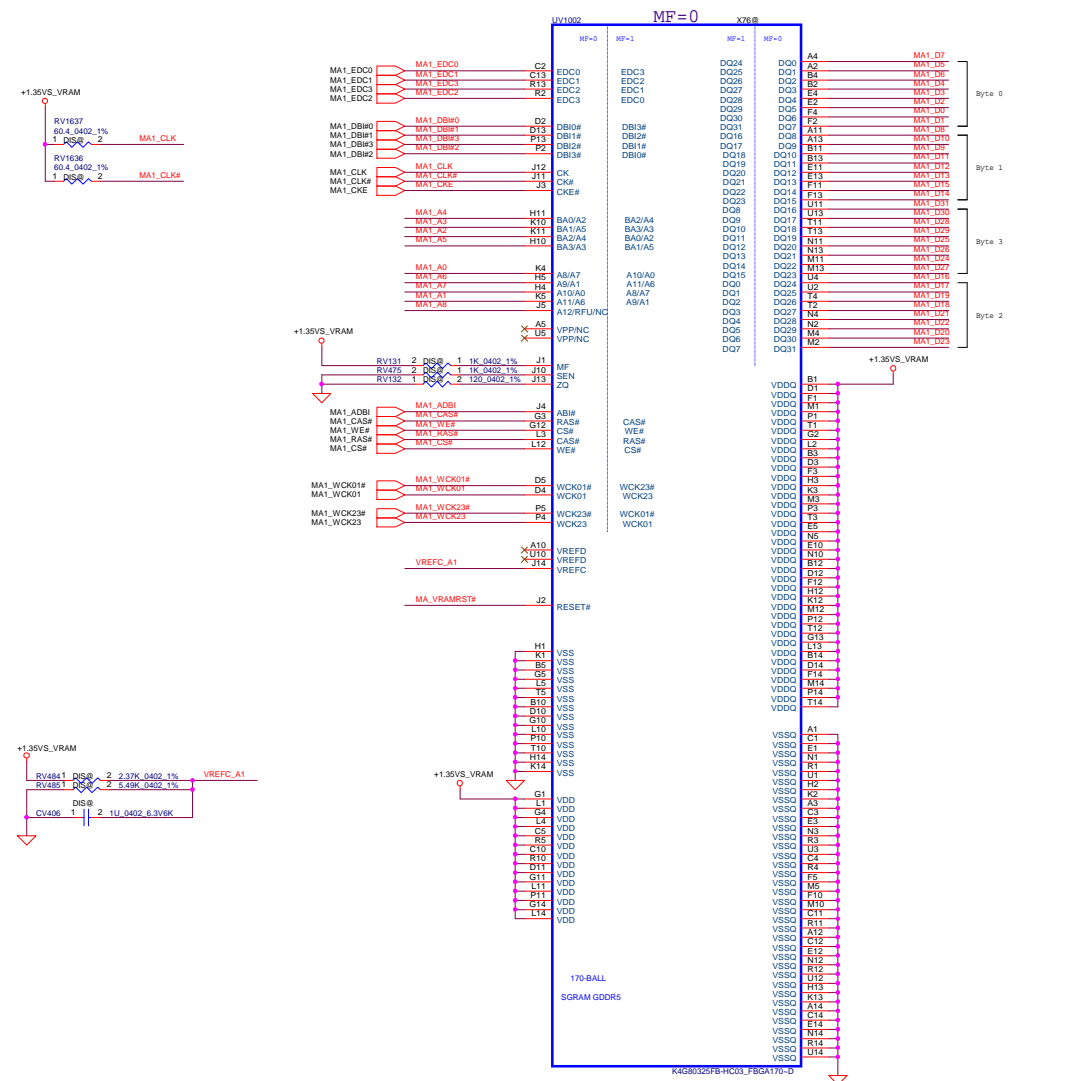
A0 Channel



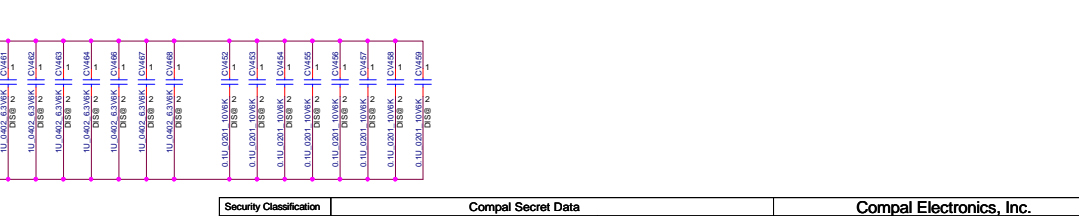
Decoupling Caps for single-sided  
1x 10uF / per DRAM  
8x 1uF / per DRAM  
8x 0.1uF / per DRAM



A1 Channel

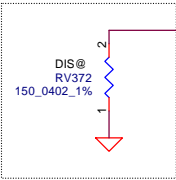
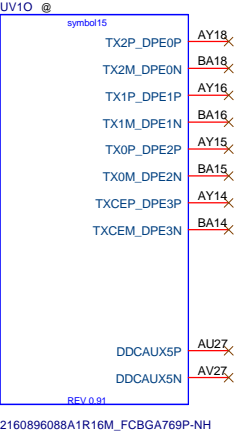


Decoupling Caps for single-sided  
1x 10uF / per DRAM  
8x 1uF / per DRAM  
8x 0.1uF / per DRAM

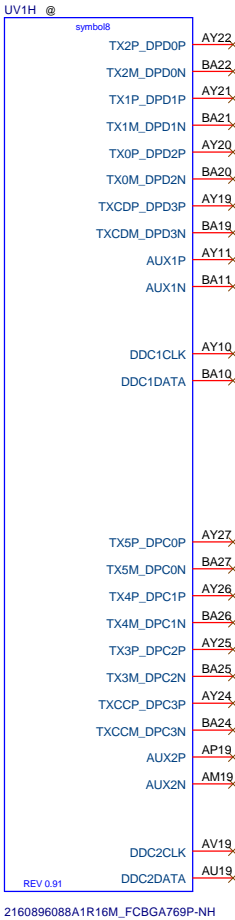
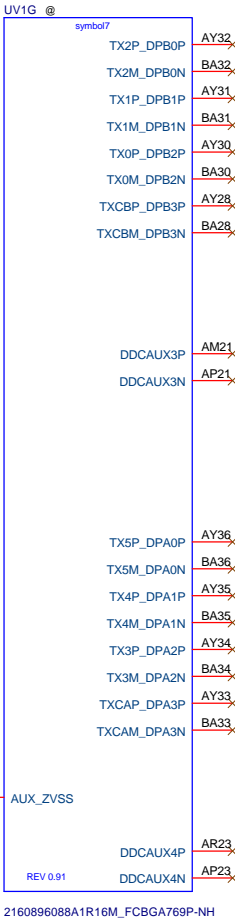


5		4		3		2		1	
D									
C									
B									
A									
		</							

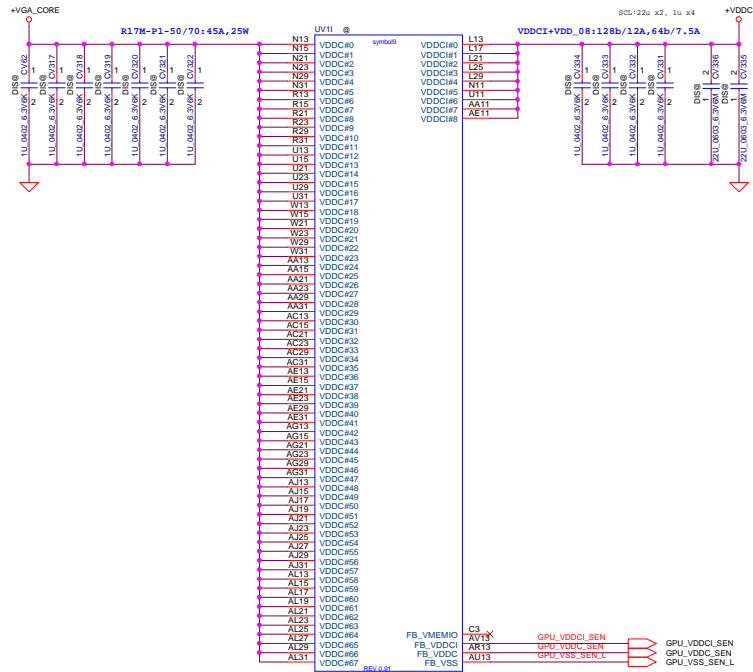
www.teknisi-indonesia.com



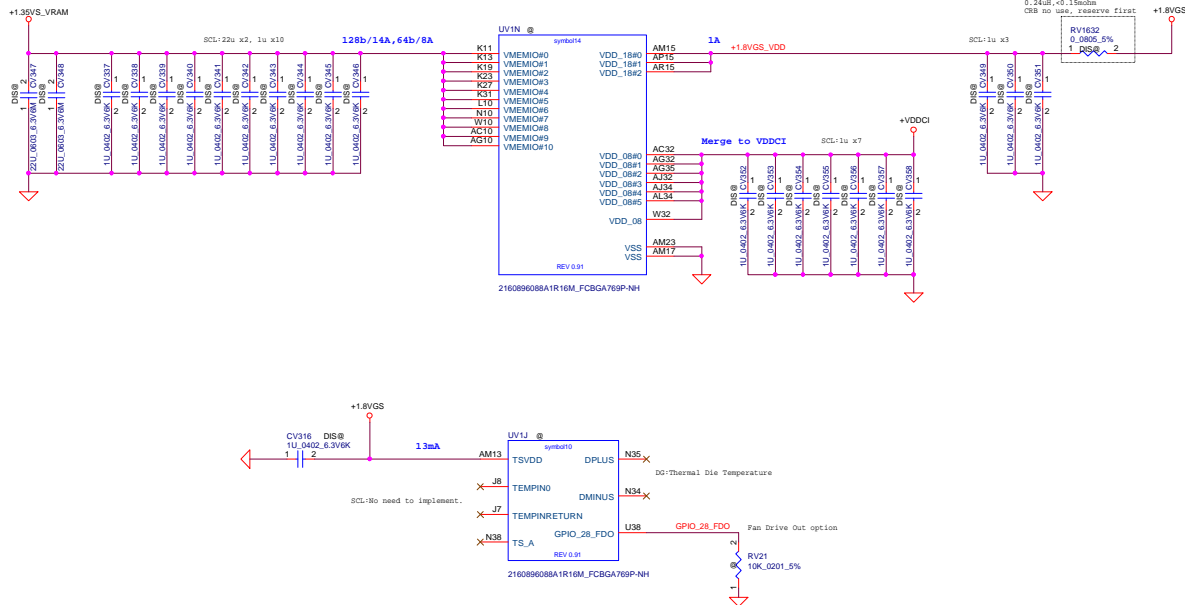
Data Book: need config even if not use display function



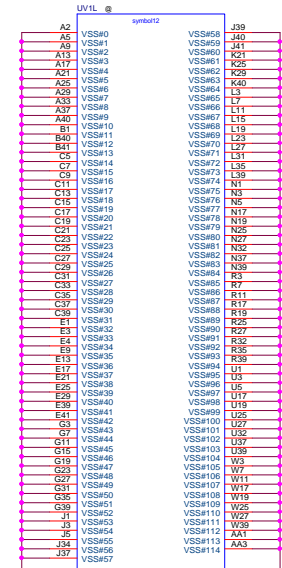
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Issued Date	2017/04/18	Deciphered Date	2019/04/18	Title	
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Size	Custom	Document Number	LA-F485P	Rev	1.A
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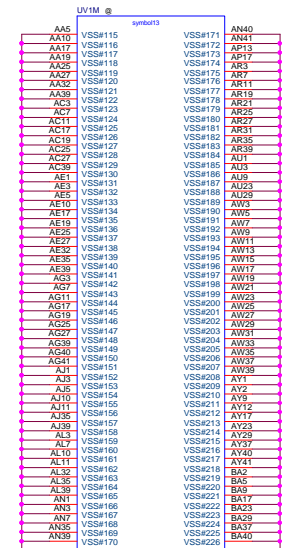
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216089608A1R16M\_FCBGA769P-NH



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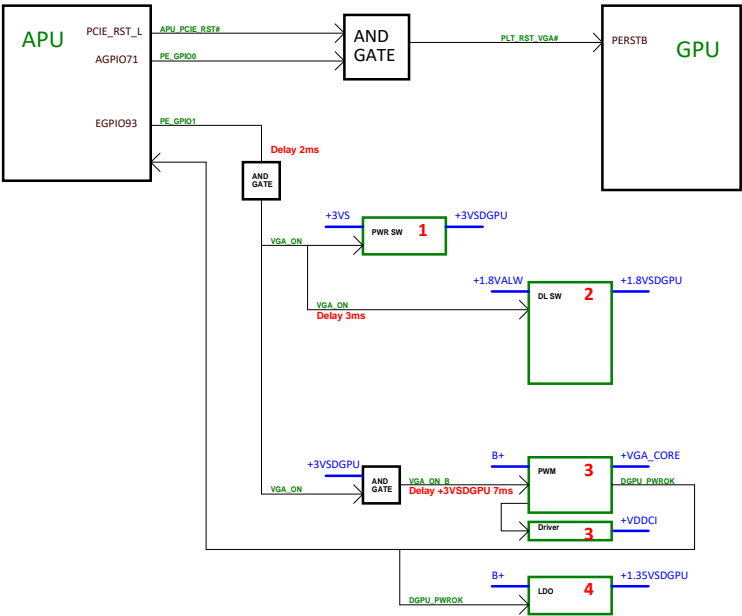
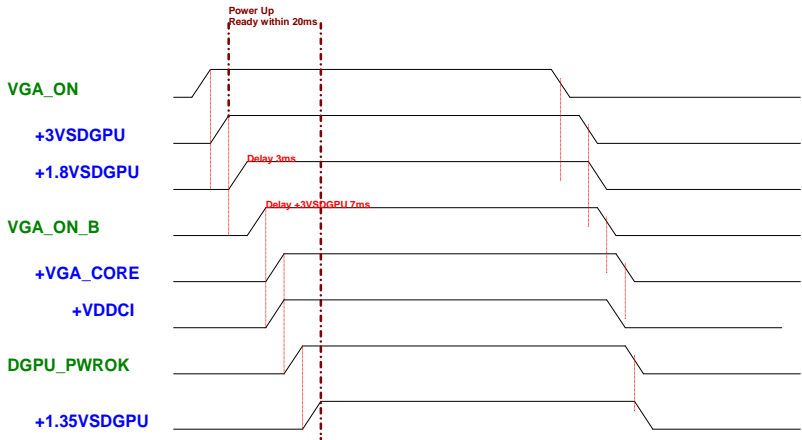


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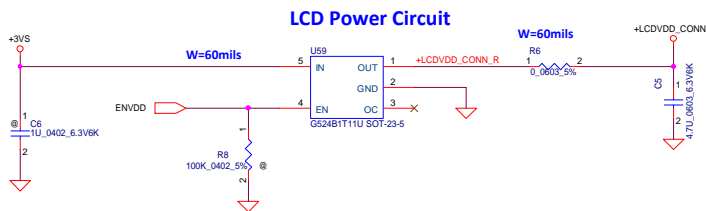
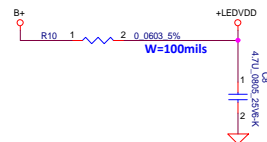
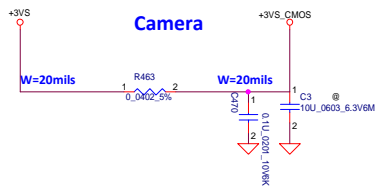
5.3 Power-up/down Sequence

"R17M-P1-50 / R17M-P1-70" has the following requirements with regards to power-supply sequencing to avoid damaging the GPU:

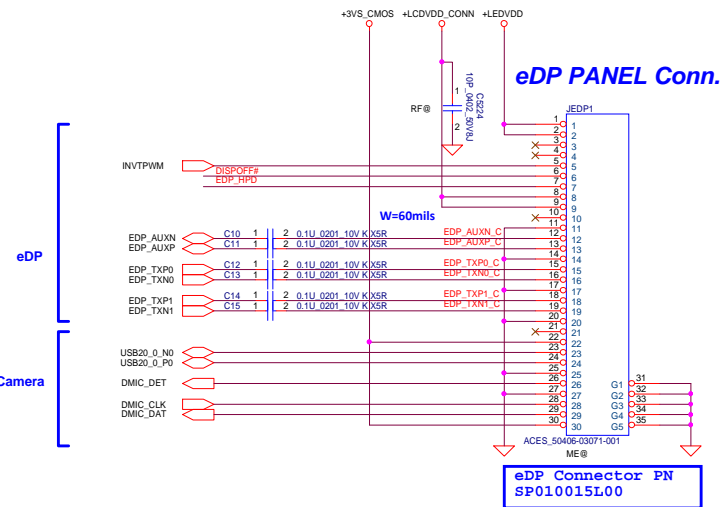
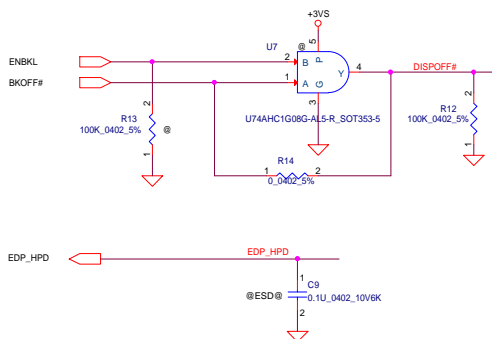
- All the GPU supplies, except for VDD\_33, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 20 mV/μs.
- It is recommended that the 3.3-V rail ramps up first.
- The 1.8 rail must reach its steady state at least 10 μs before VDDC, VDDCI, VDD\_08, and VMEMIO start to ramp up.





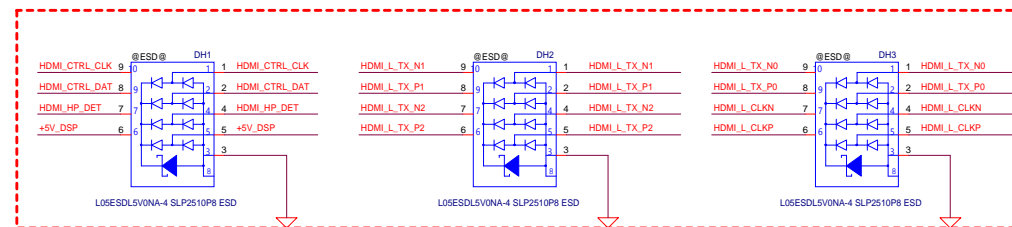
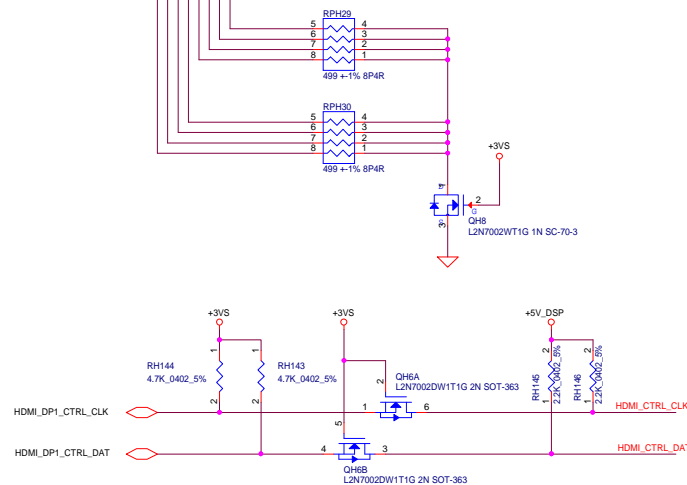
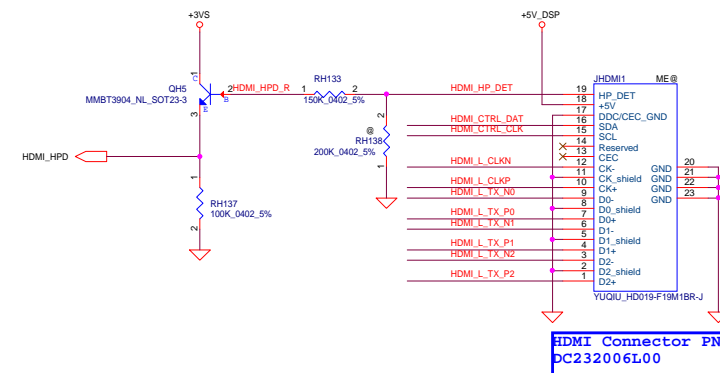
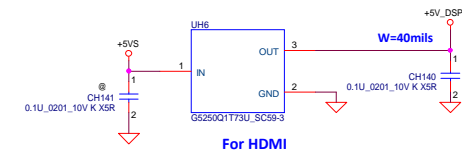
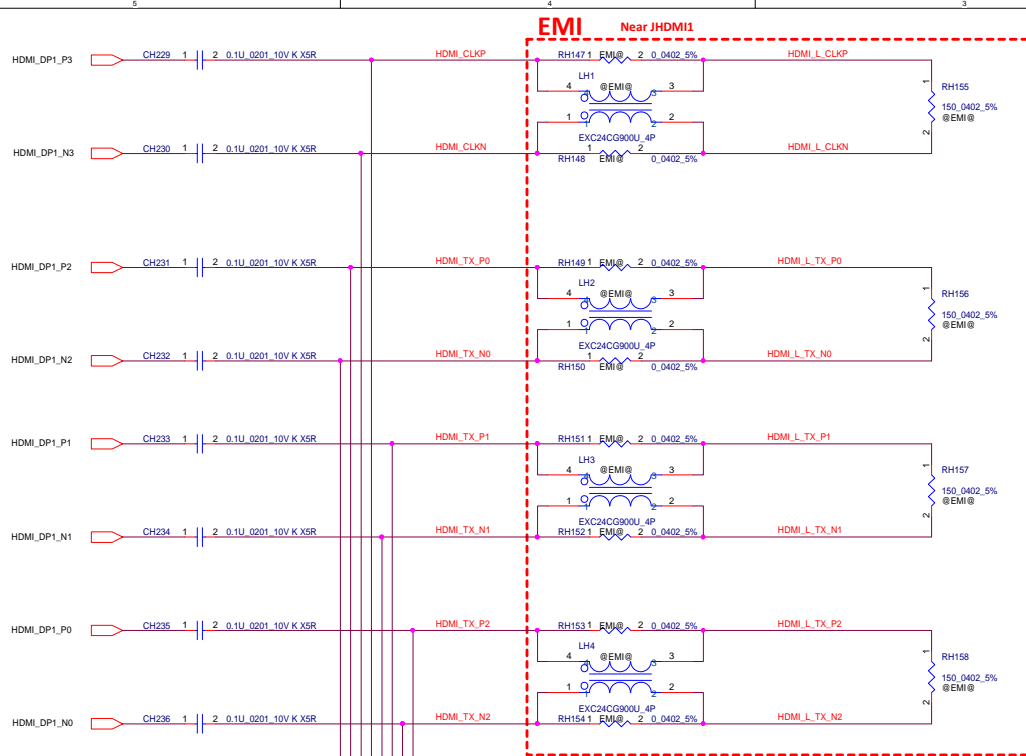


From PCH  
From EC

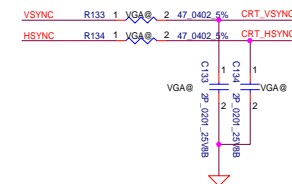
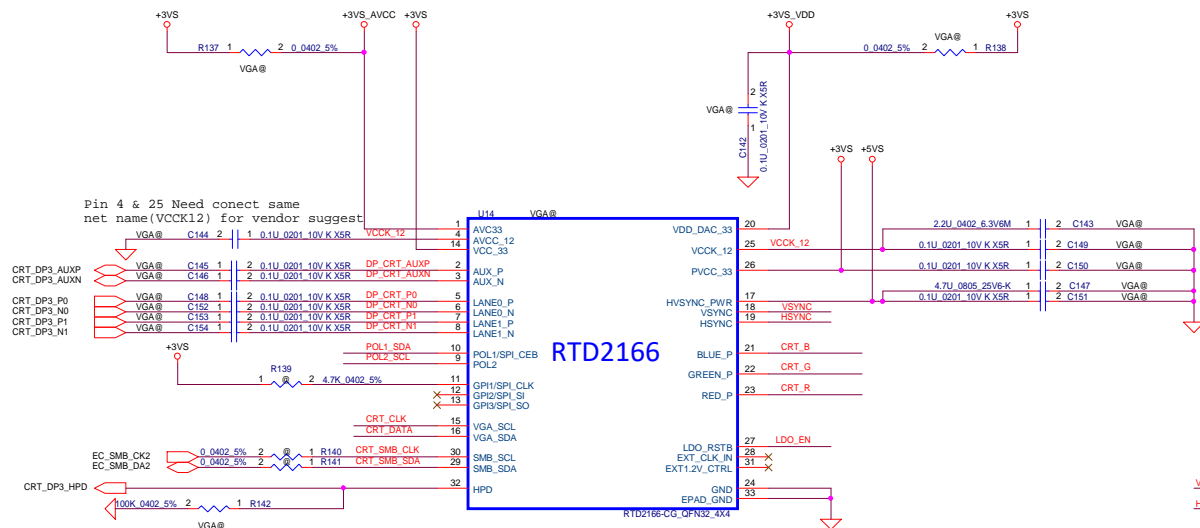


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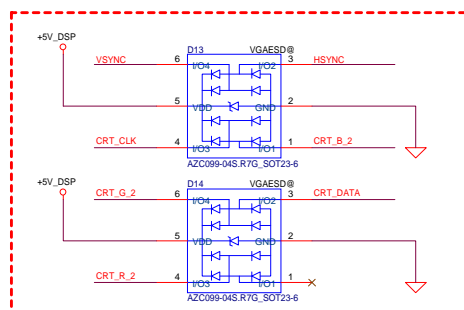




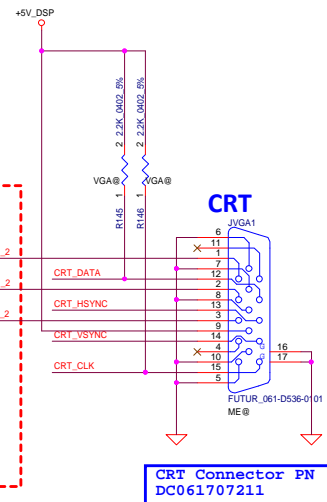
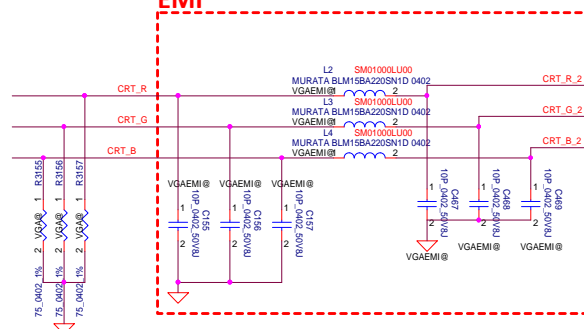
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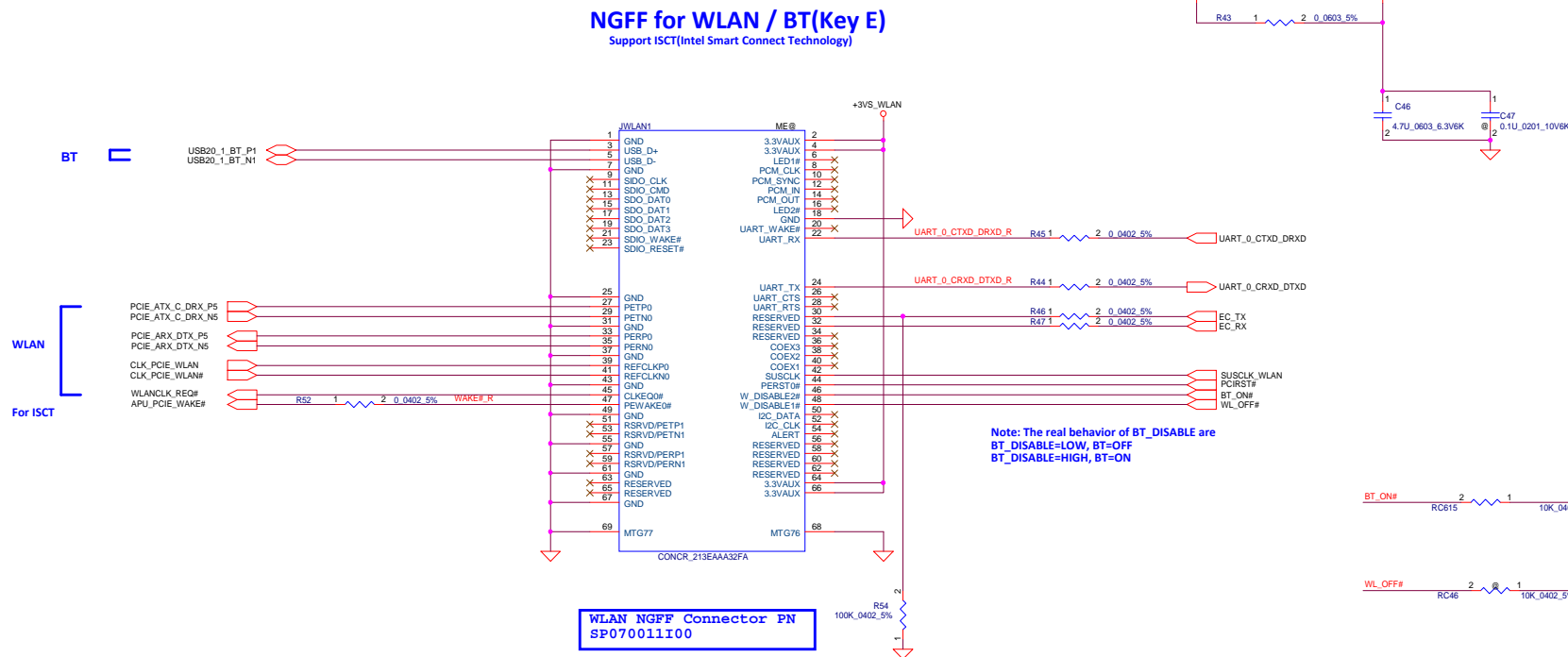
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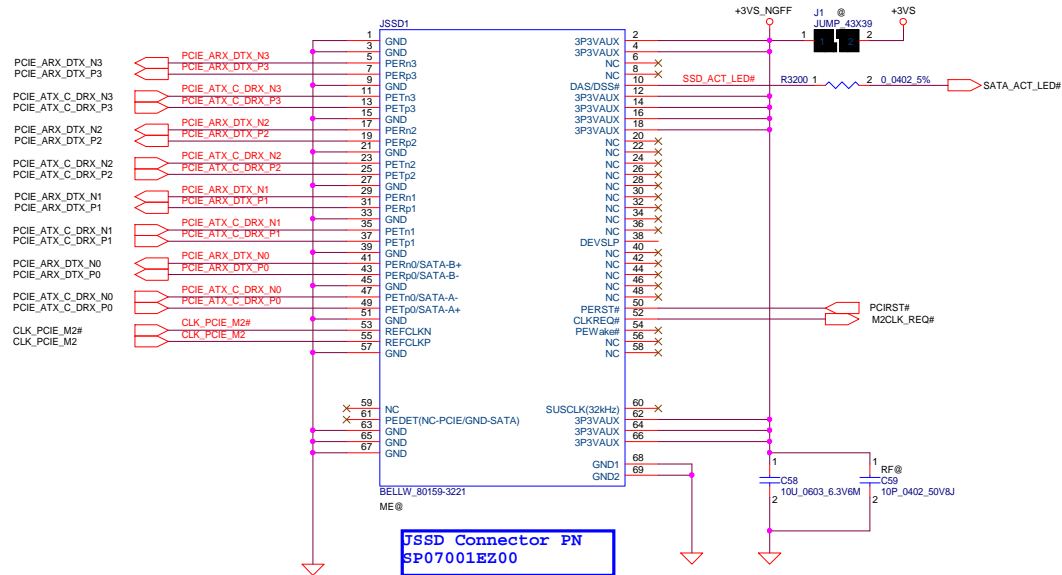
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Date:				Friday, August 11, 2017	Sheet 26 of 54

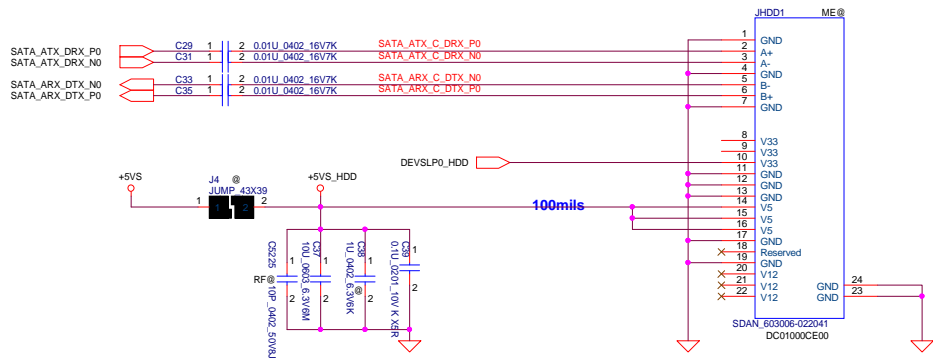


M.2 mSATA Conn

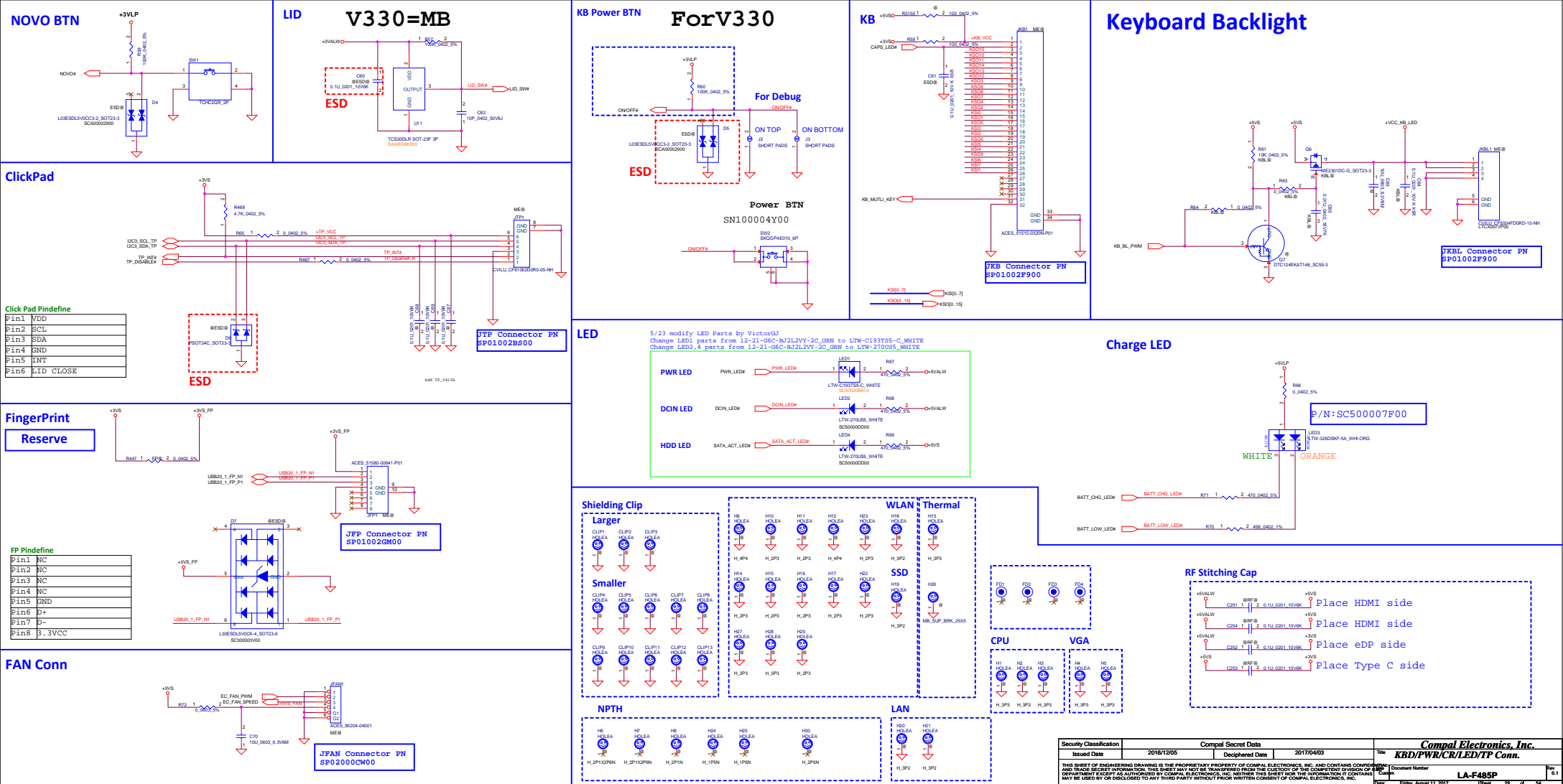


HDD

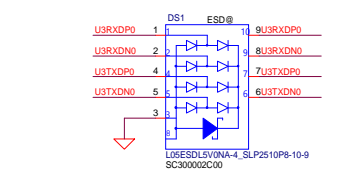
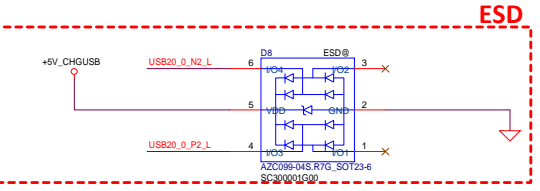
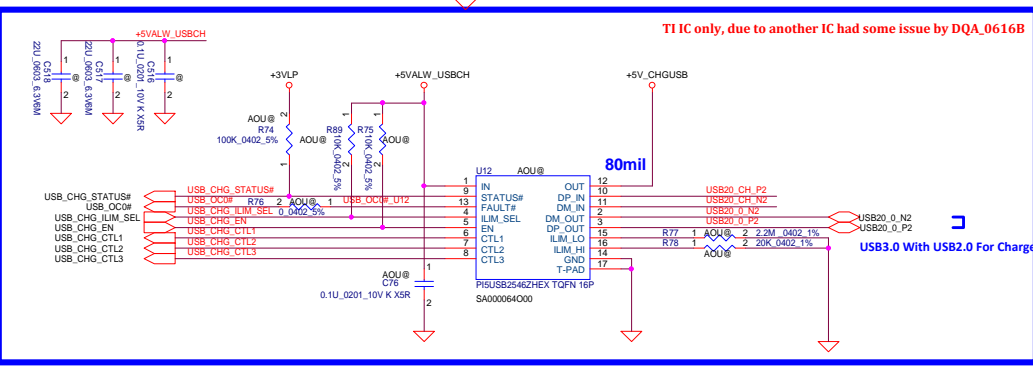
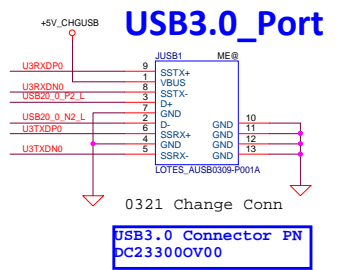
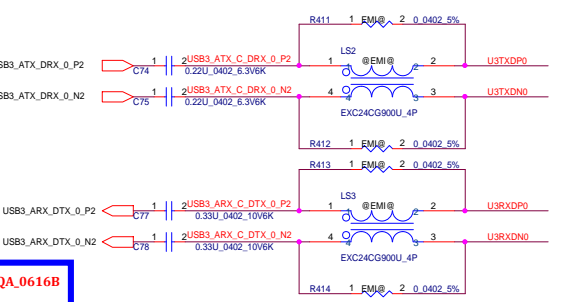
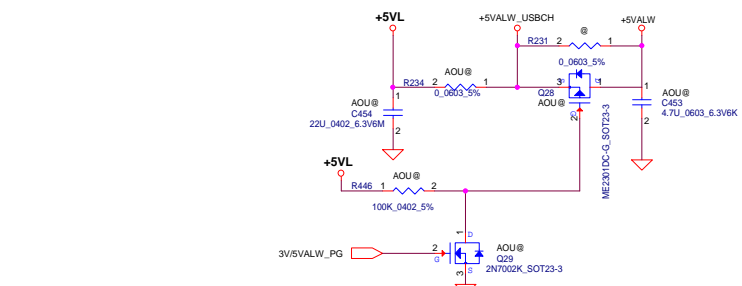
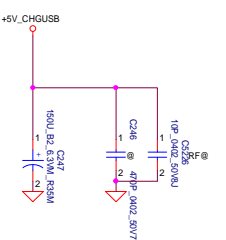
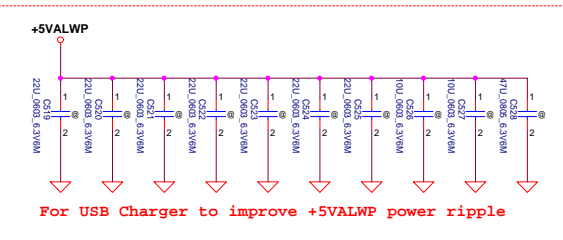
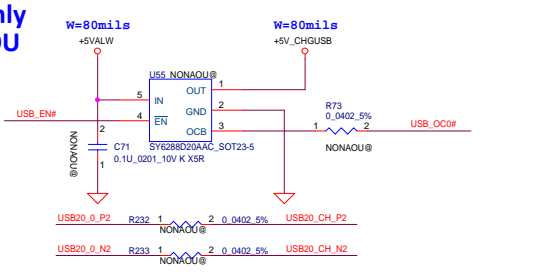
SATA HDD Conn.



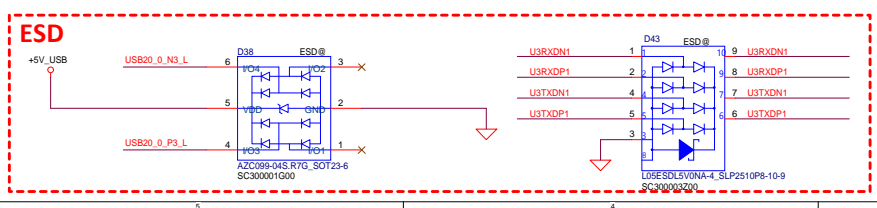
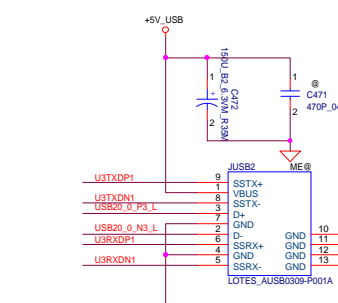
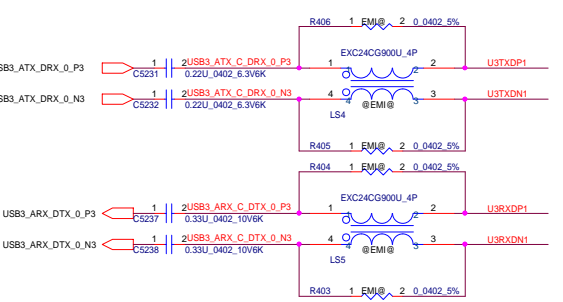
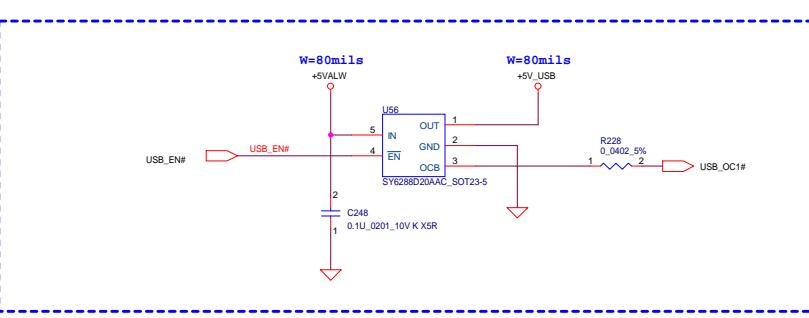
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USB 3.0 V330 only NONAOU

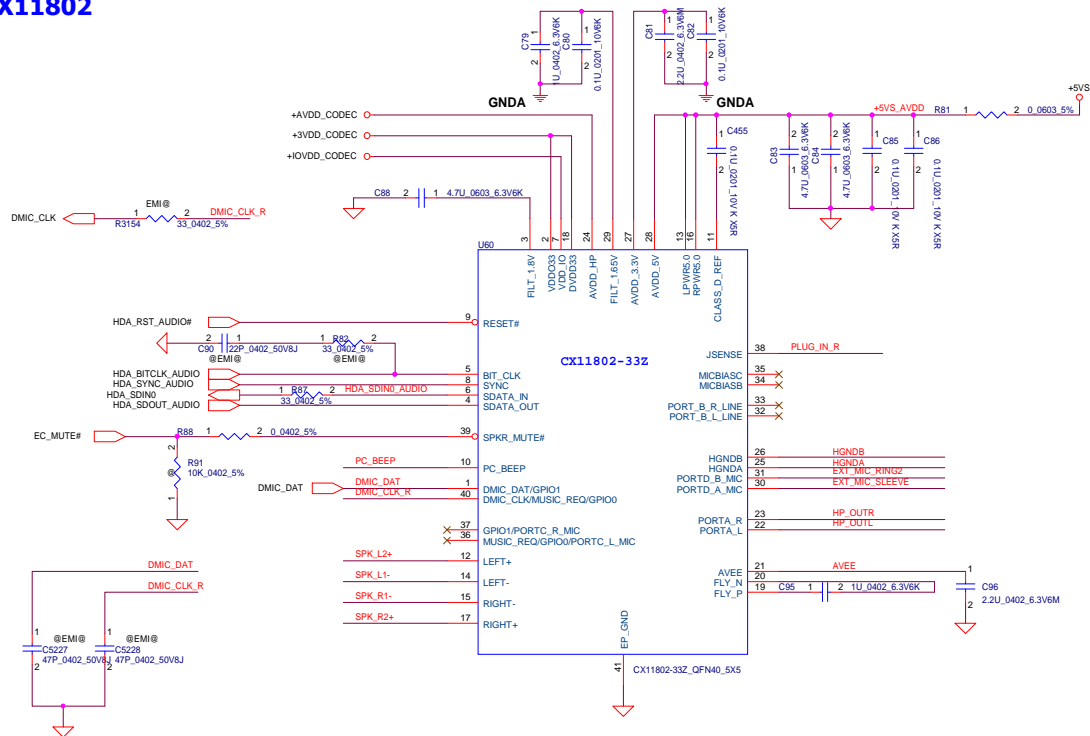


USB 3.0 Right side

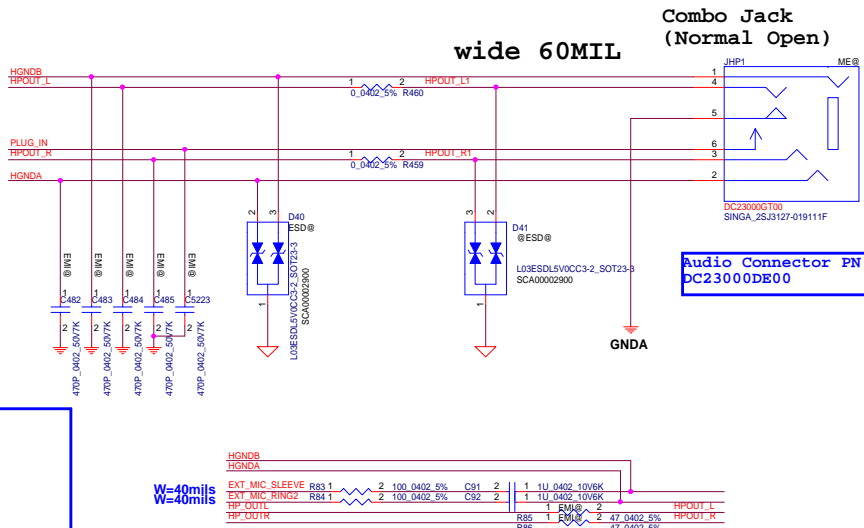


Title			
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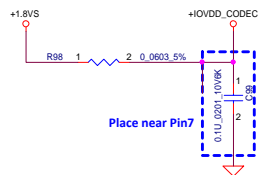
# CX11802



## Combo Jack

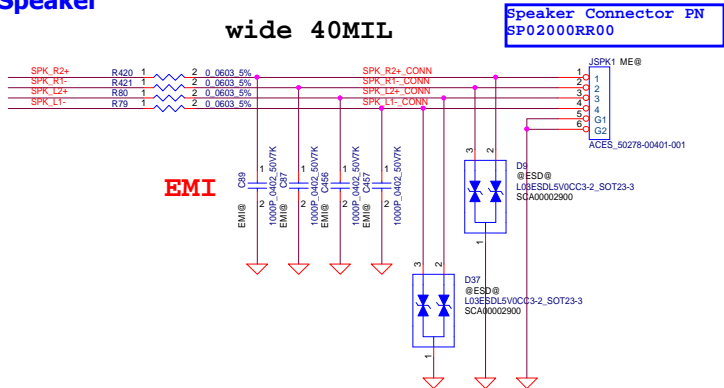


**+1.8VS → +IOVDD\_CODEC**

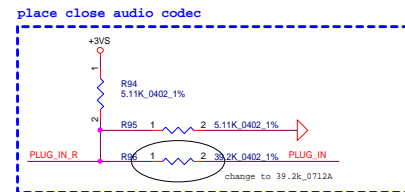


**Speaker**

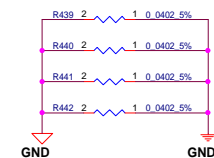
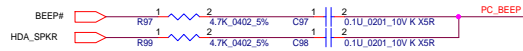
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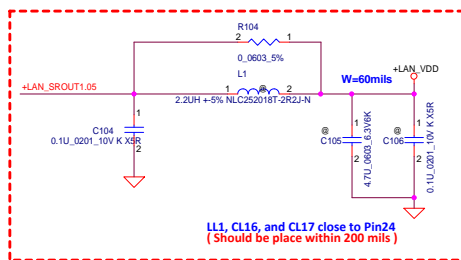
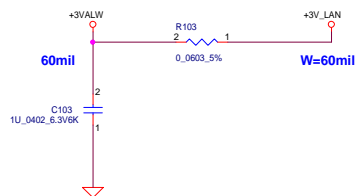
Speaker Connector PN  
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## PC Beep

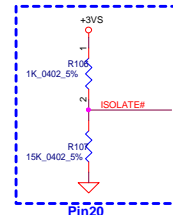
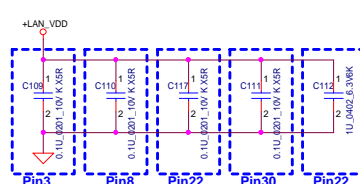
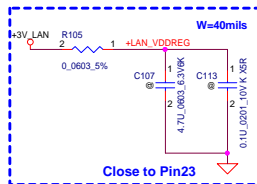
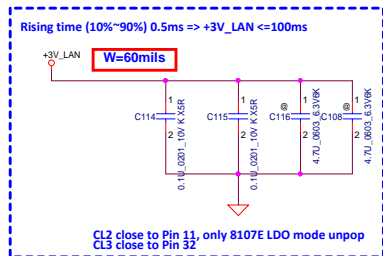


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				Size C		Document Number
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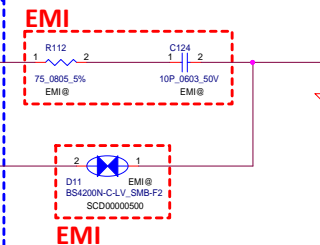
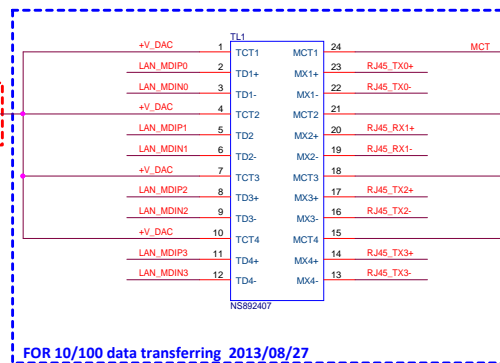
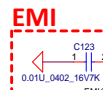
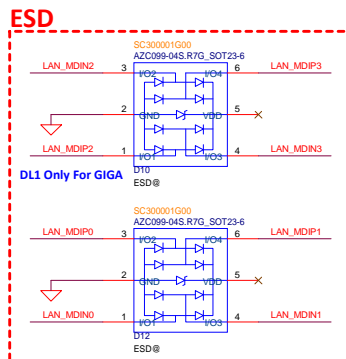
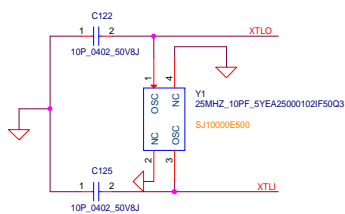
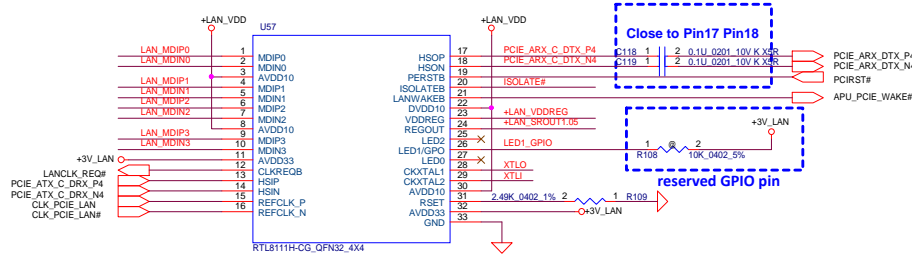
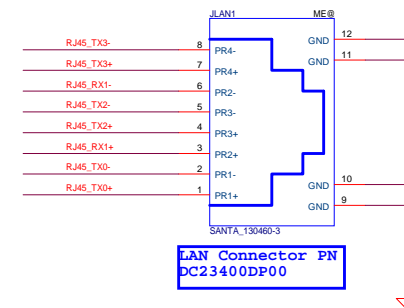


1.0V Source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
RTL8111H	LDO	X	X	O	O

Please refer to the table above when using different 1.0V supply source.



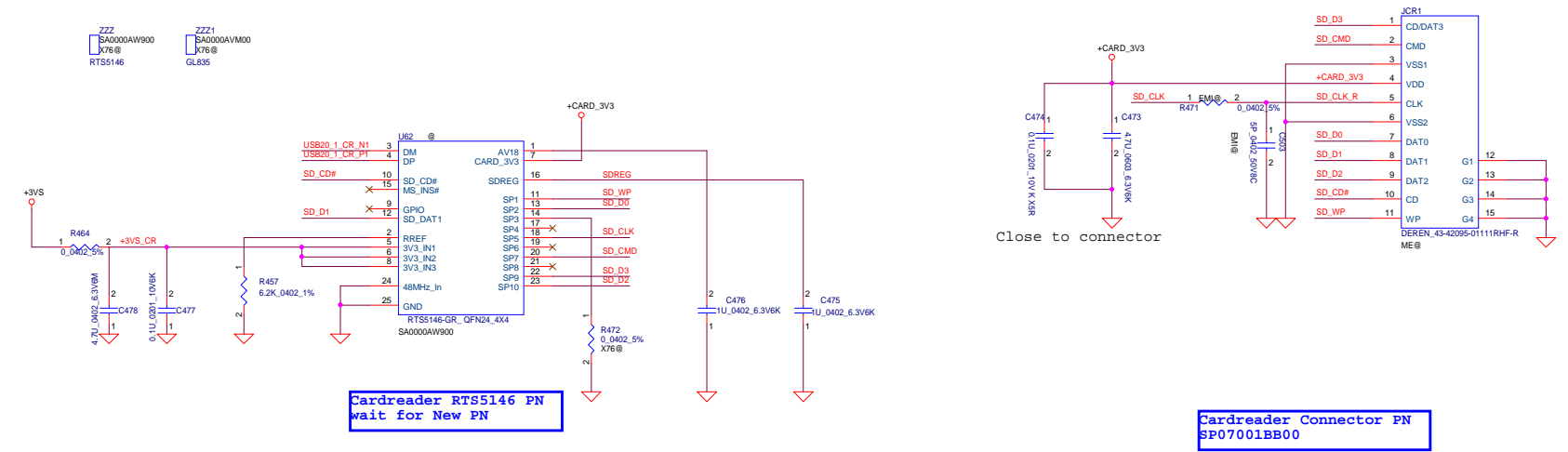
## RJ-45 CONN.



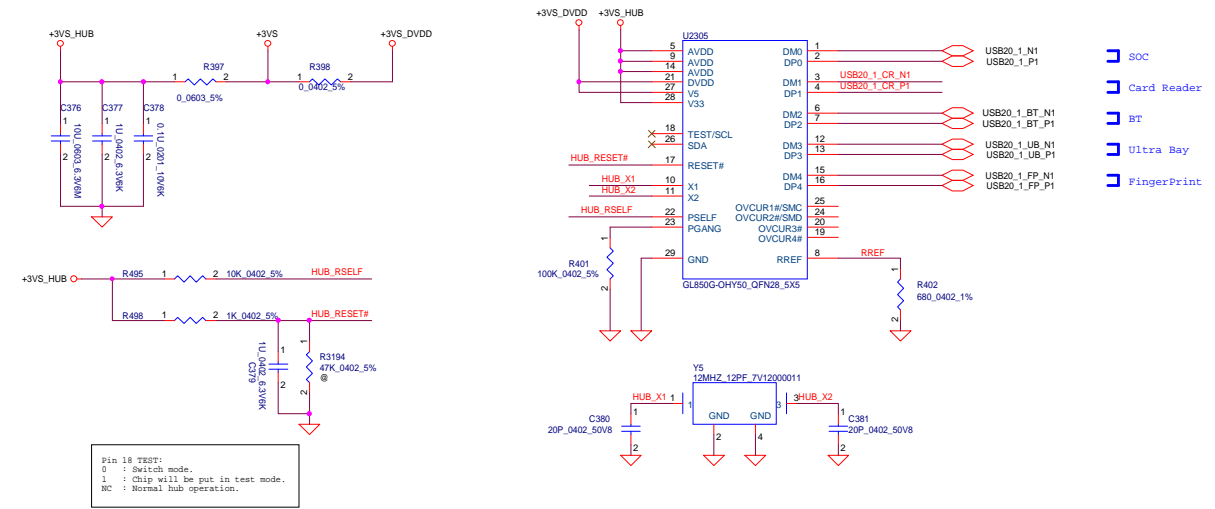
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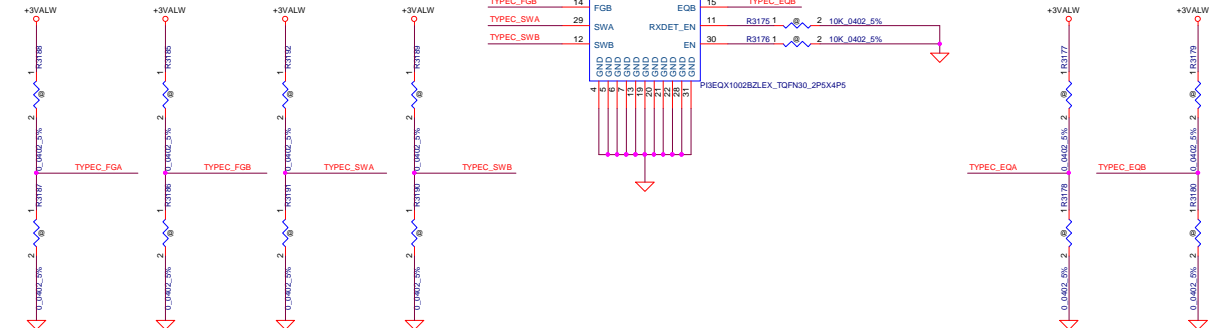
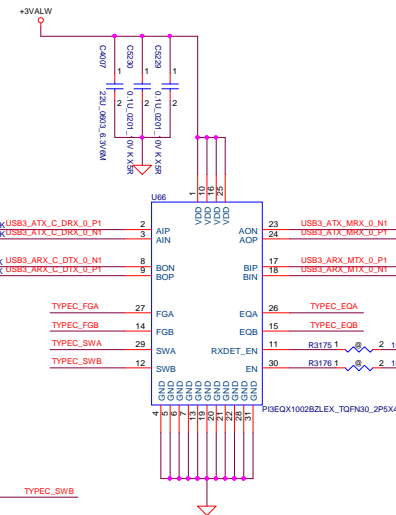
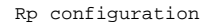
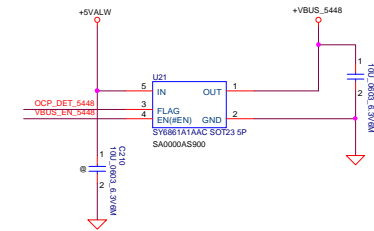


CardReader



USB20 HUB



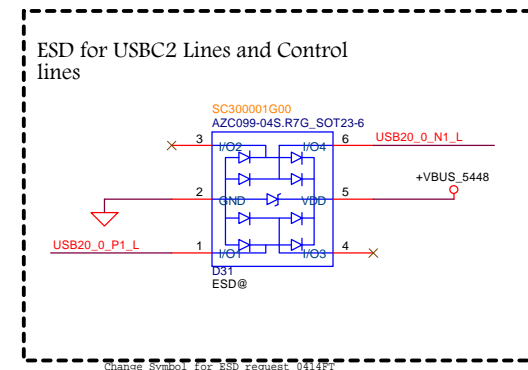
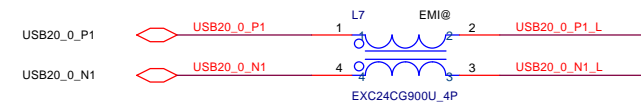
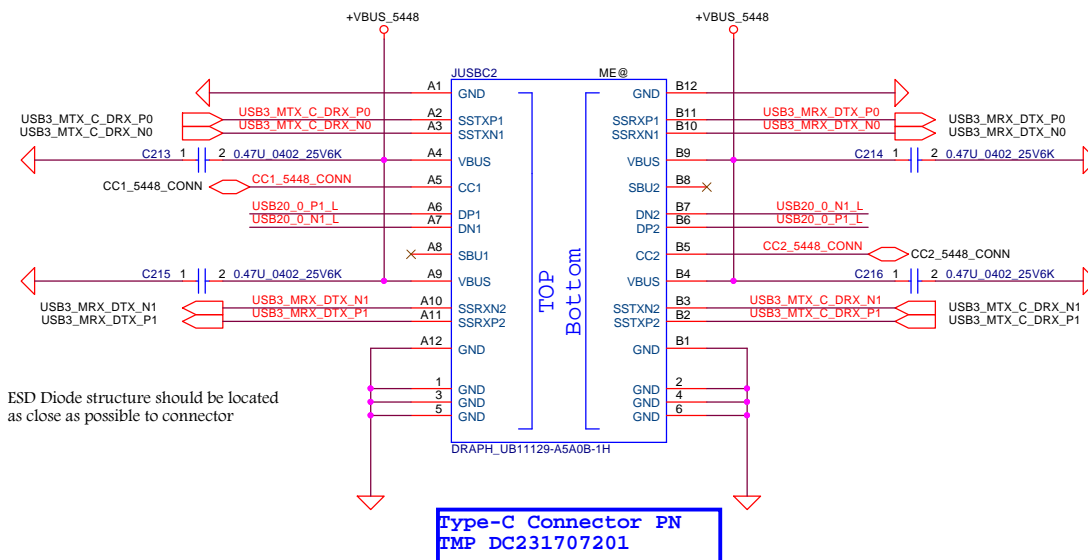


Power switch enable pin	Note	
Low Active	R190/R187 mount	Pull Up & Down
High Active	R190 mount R187 don't mount	Pull Down

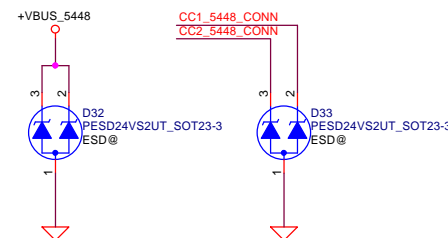
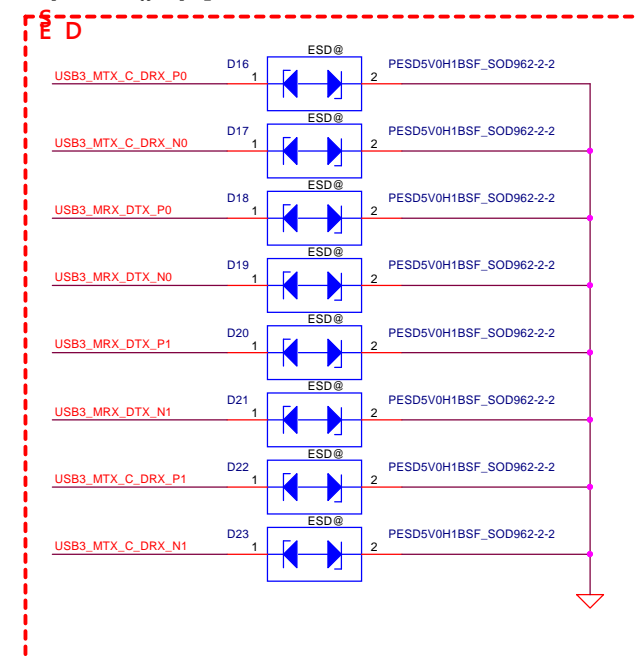
  

Power switch OCF pin	Note	
Low Active	R191/R188 mount	Pull Up & Down
High Active	R191 mount, R188 don't mount	Pull Down

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			Date:	<b>LA-F485P</b>	
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Change Diode for Type-C gen2\_0525B

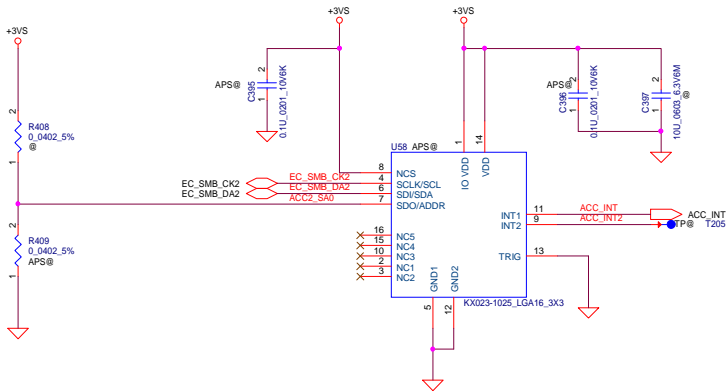


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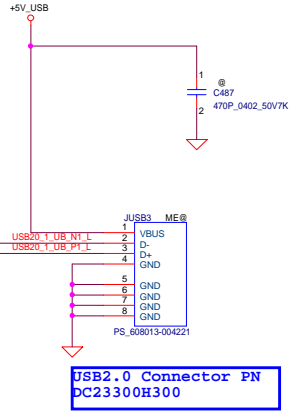
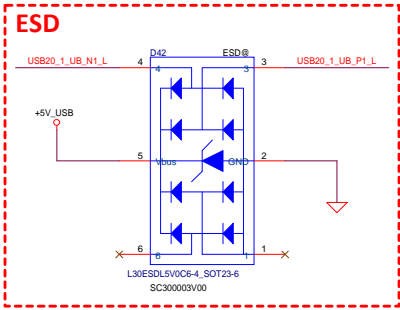
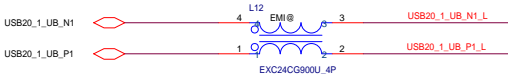
APS G-Sensor

Kionix KX023-1025

SDO/ADDR	Address R/W
VDD	3Fh/3Eh
VSS	3Dh/3Ch



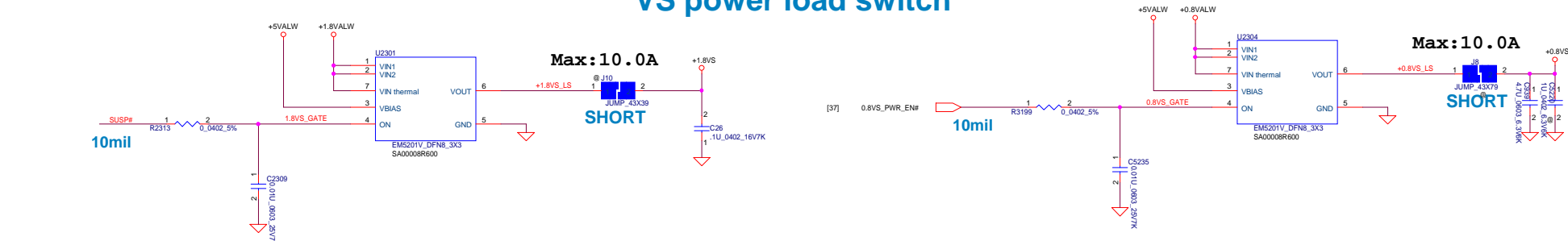
2nd Battery USB2\_CONN



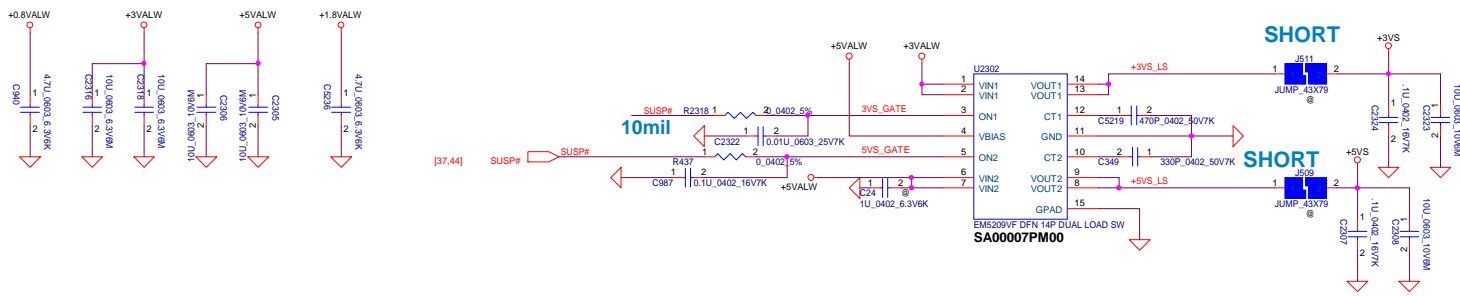


Main Func = DC Interface

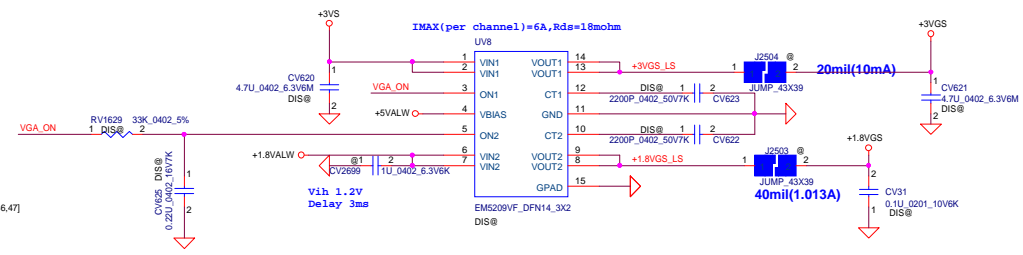
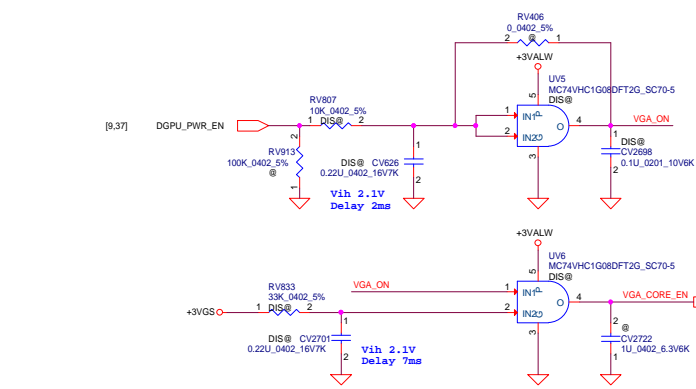
VS power load switch

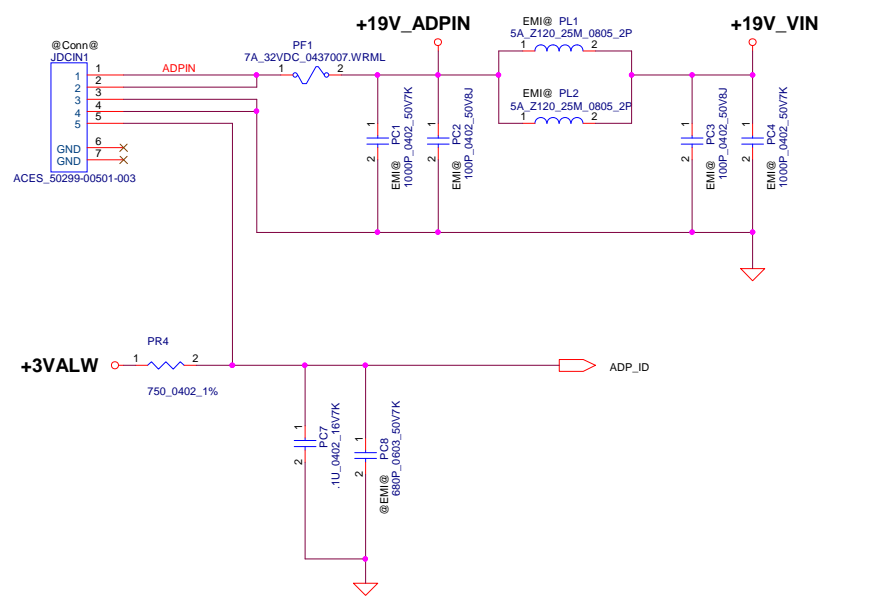


Max: 5.07A



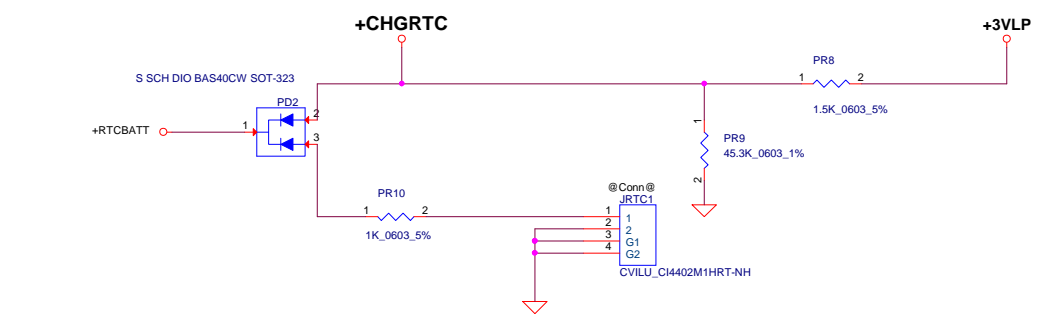
dGPU power load switch





BOM Structure Table

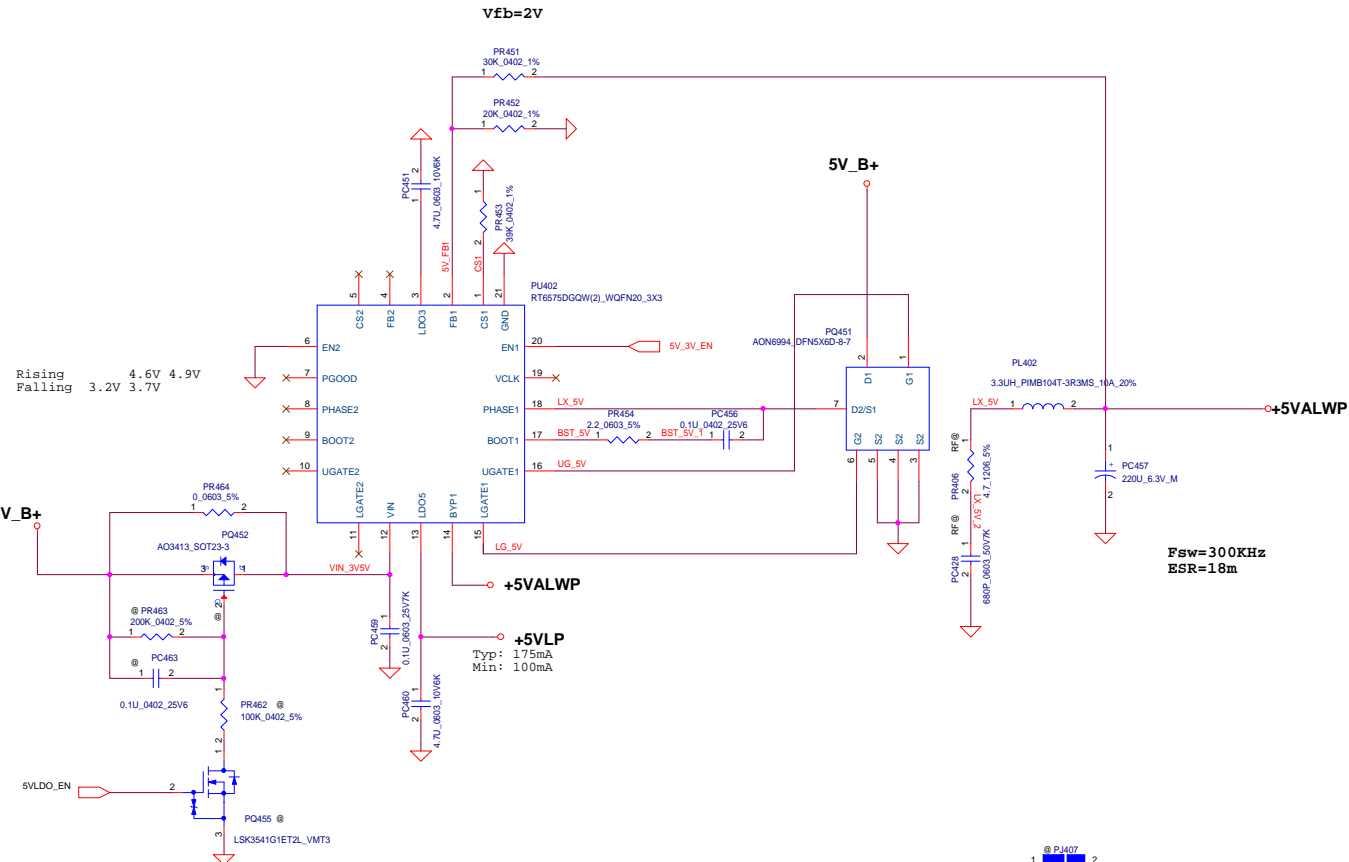
Item	BOM Structure
Support Type-C PD	PD@
For EMI	EMI@
For RF	RF@
For DIS	VGA@
For DIS of EMI	VGA_EMI@
For DIS of RF	VGA_RF@





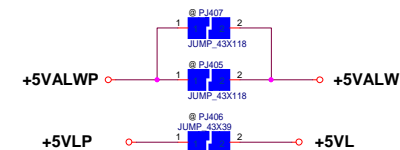
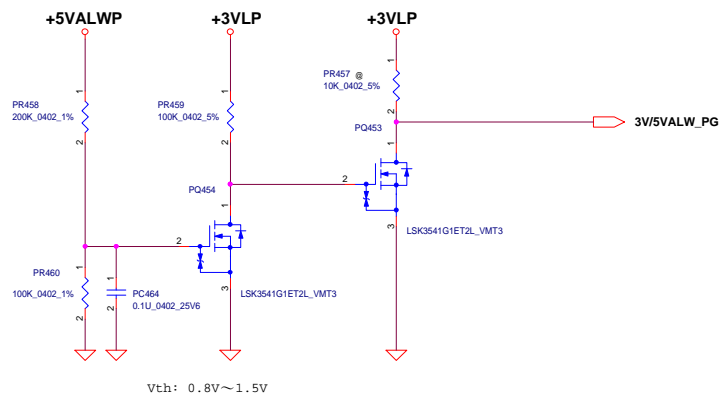




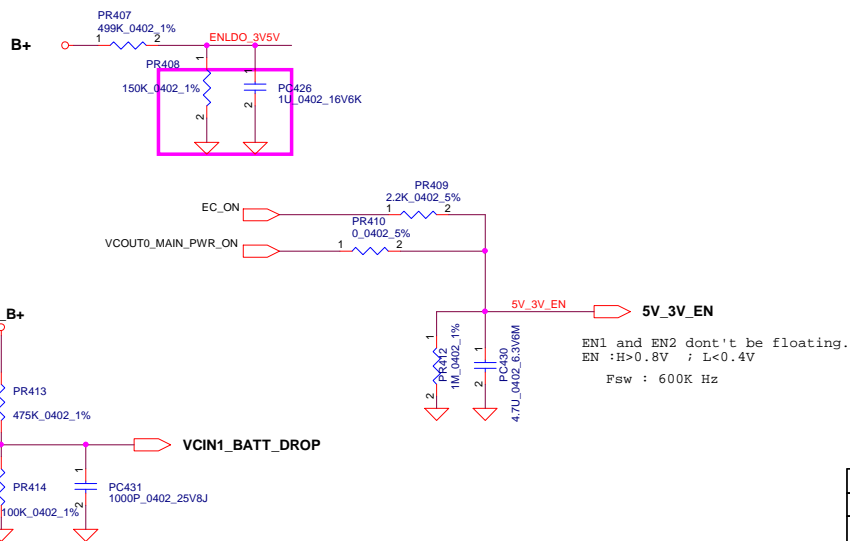
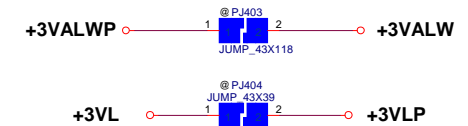
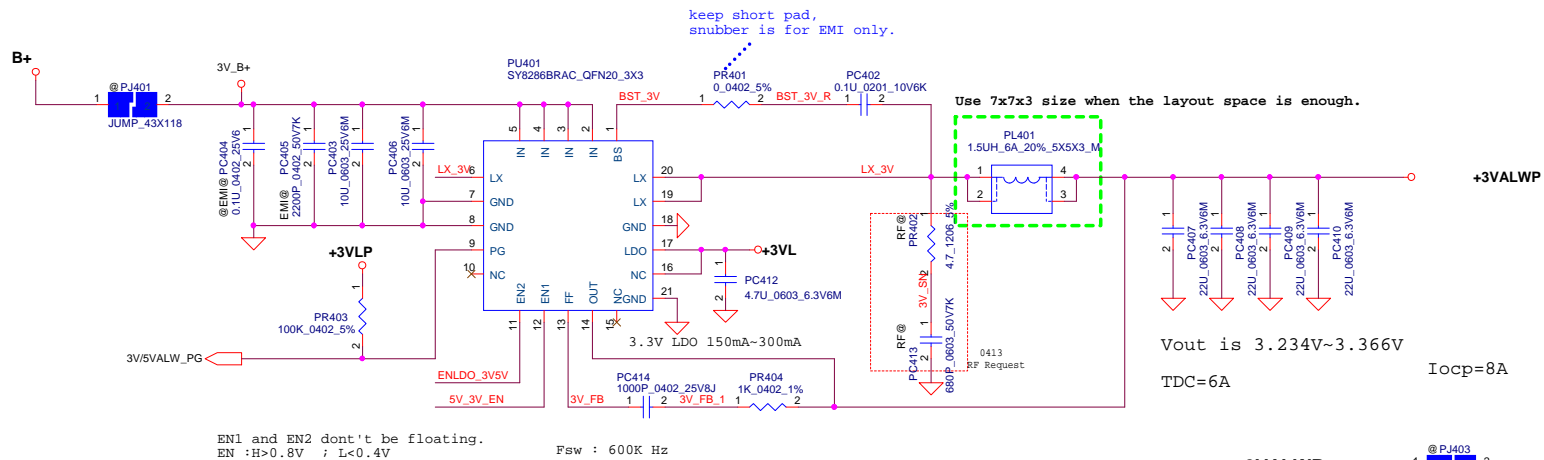


$$\begin{aligned} V_{out} &= V_{fb} \cdot [1 + (R_t/R_b)] \\ &= 2 \cdot [1 + (30K/20K)] \\ &= 5V \end{aligned}$$

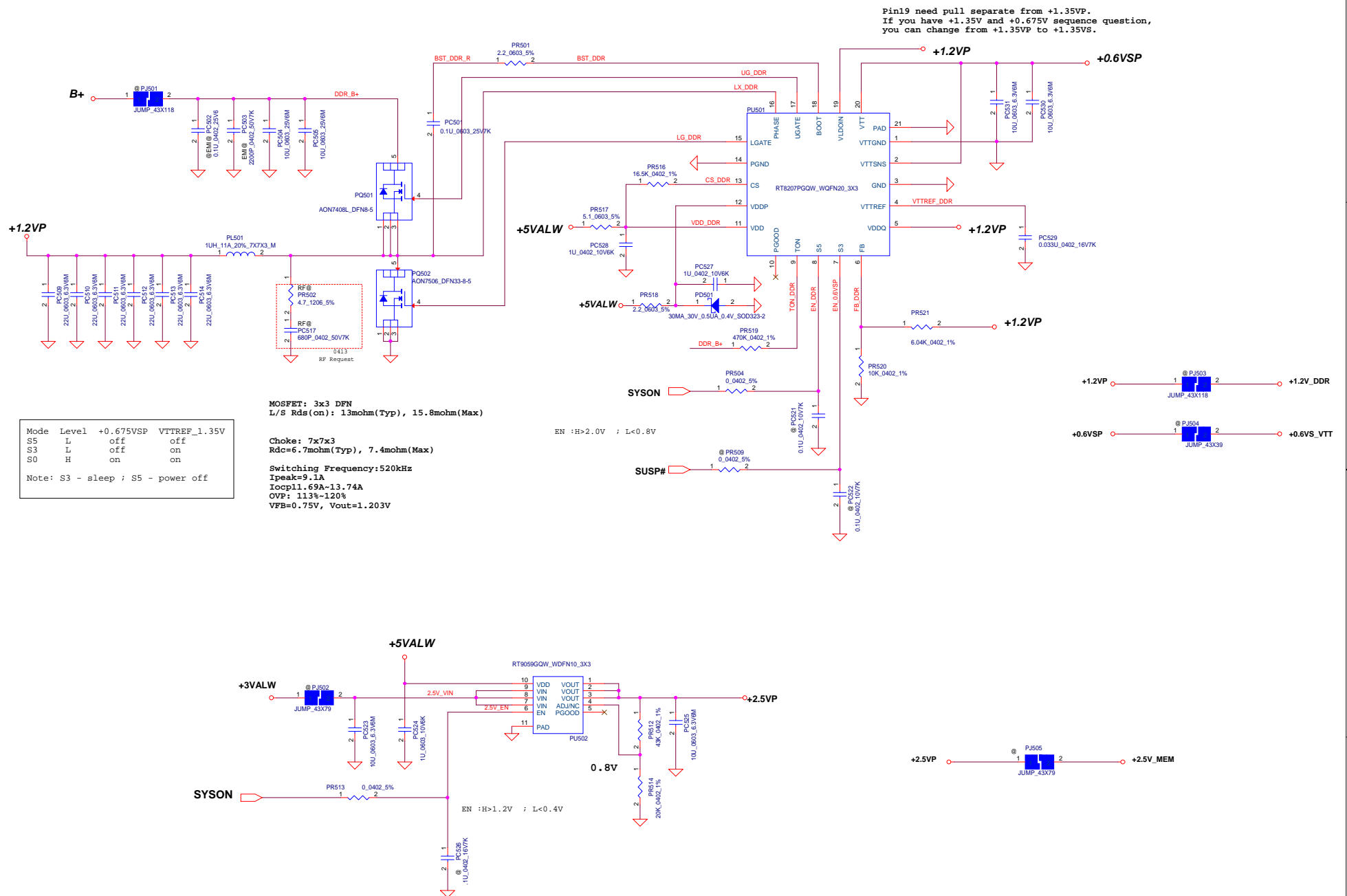
```
+5VALWP
Imax=10.5A,Ipeak=12.4A ;Fsw=300KHz
Iocp=(Rcs1*Trip)/Rdsn
Rds : L/S -> typ:2.8mohm ; max: 3.5mohm
Trip=9-11 uA
Iocp=16.49A
Output Cap. ESR=18mohm
Delta IL=(Vin-Vo)/L1*[(Vout/Vin)*T]=2.04A
```

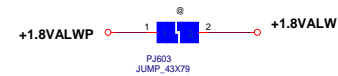
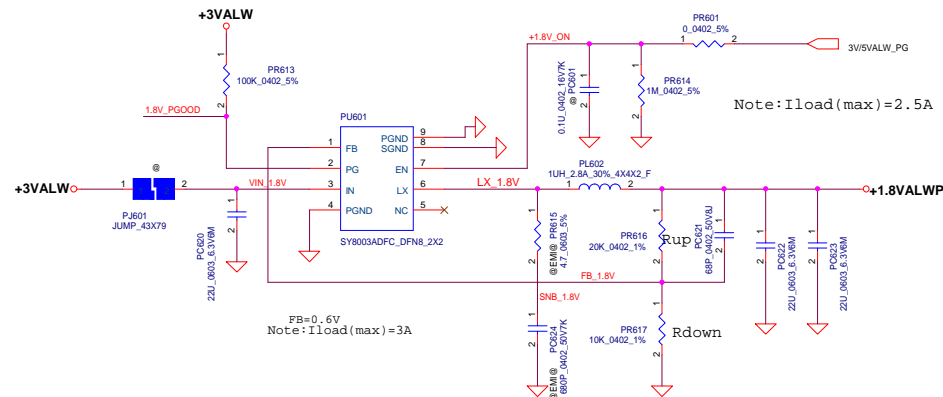


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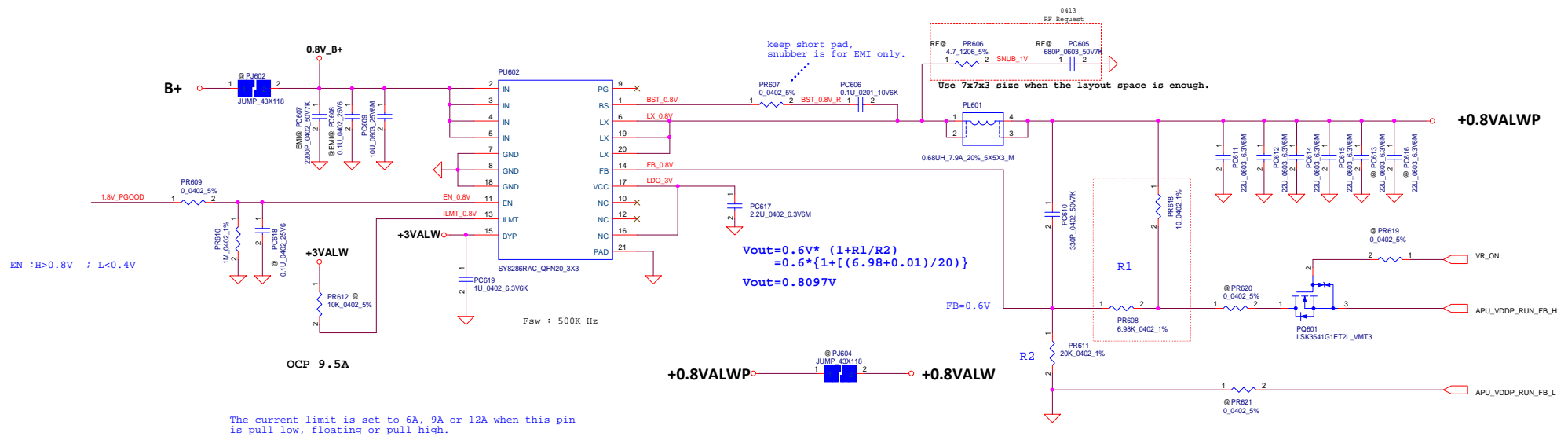




Note:  
When design Vin=5V, please stuff snubber  
to prevent Vin damage

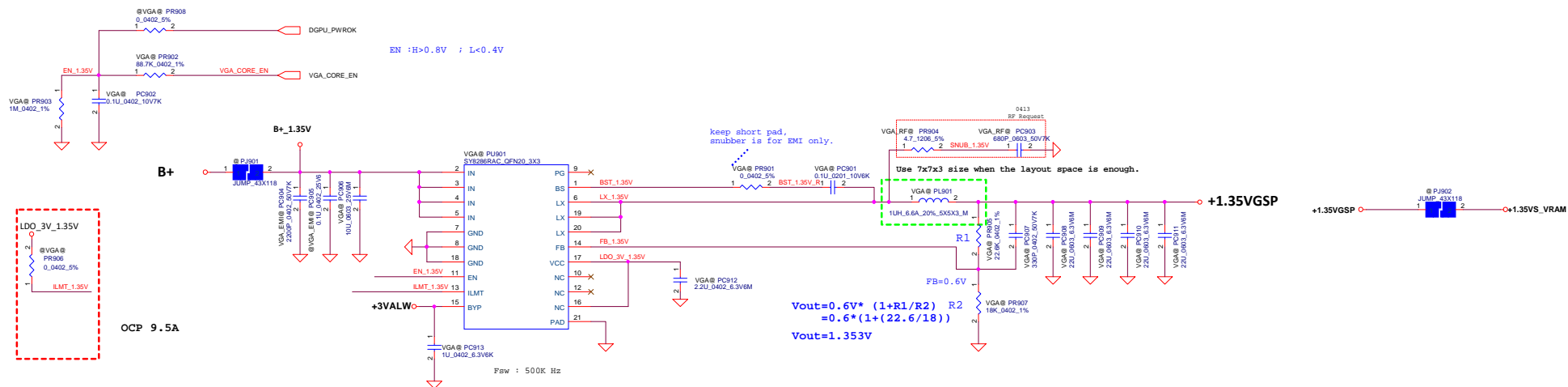
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

$$= 0.6 * (1 + 20/10) = 1.8V$$

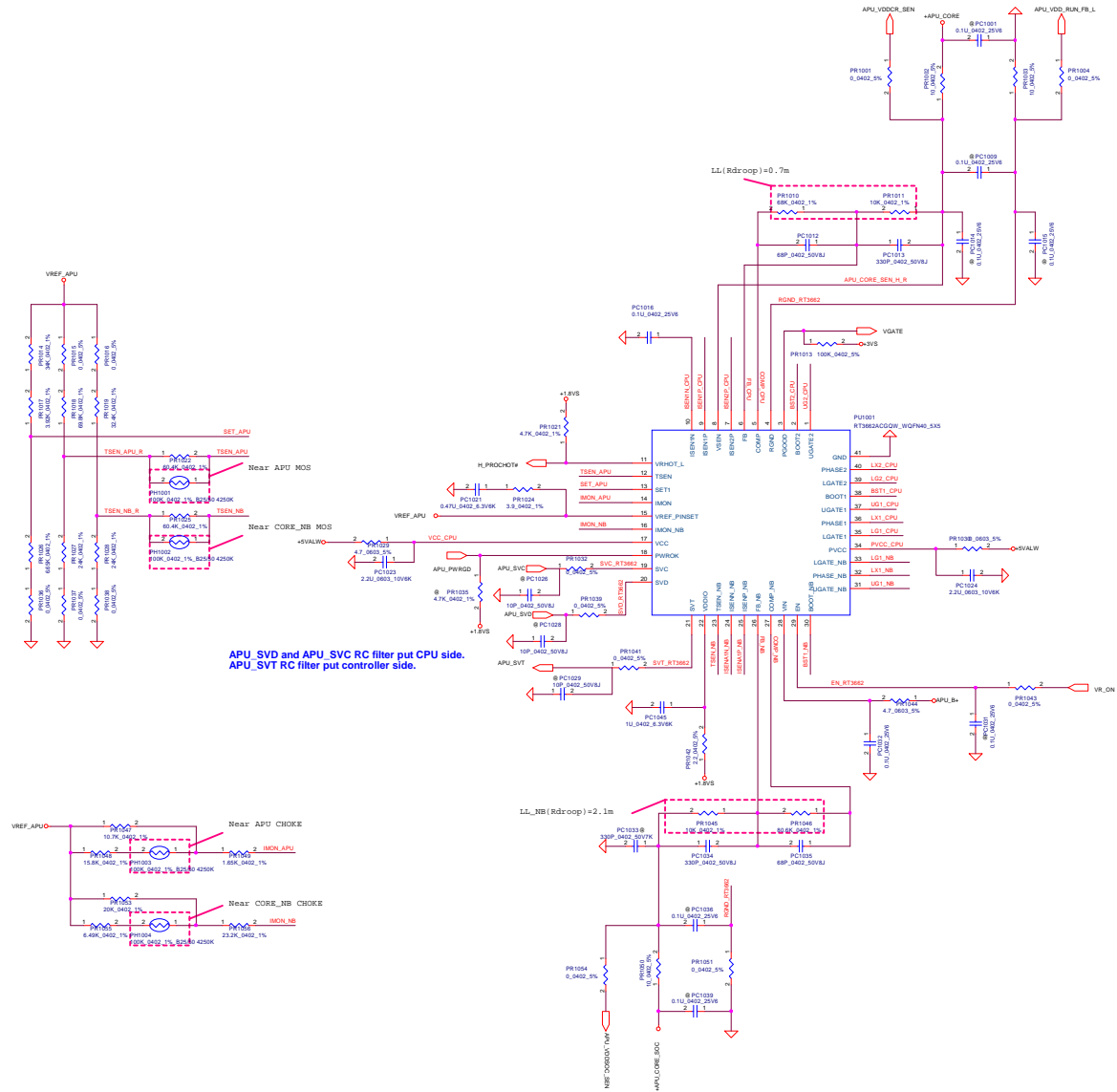


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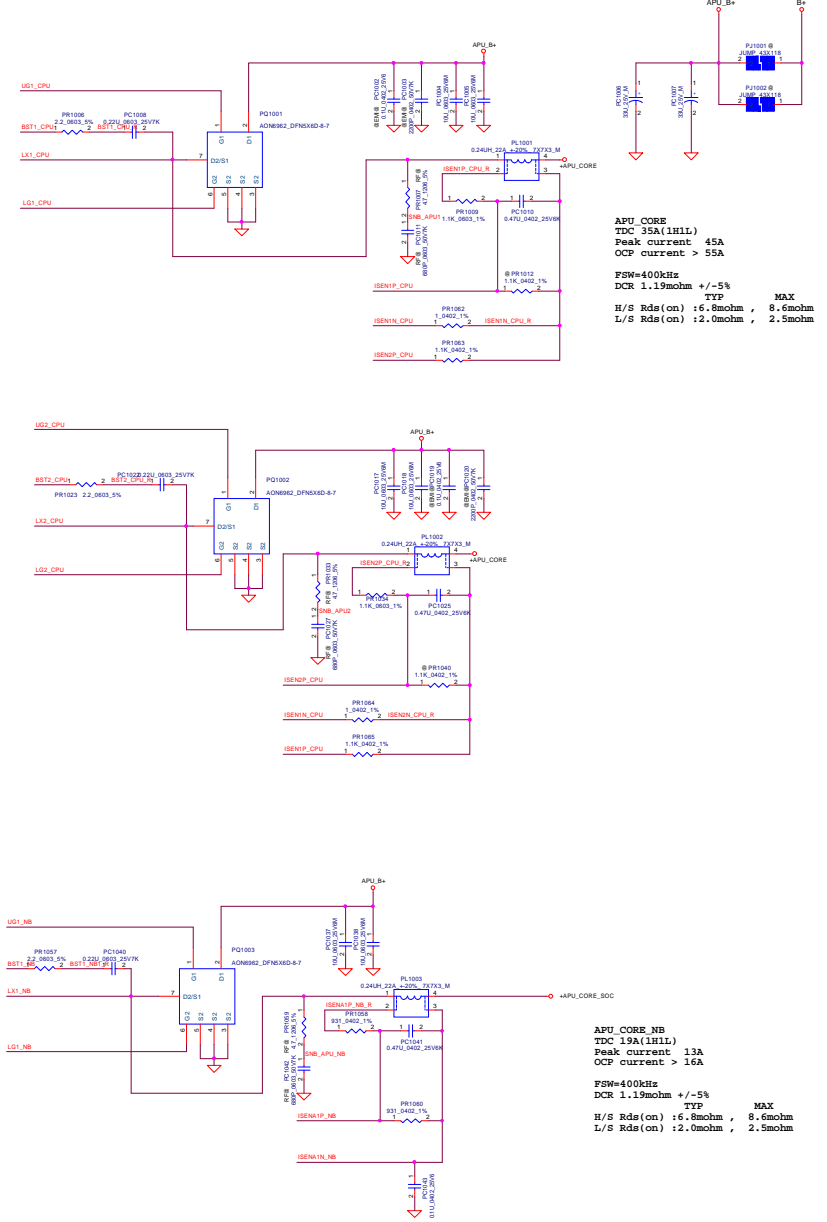
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APU\_SVD and APU\_SVC RC filter put CPU side.  
APU\_SVT RC filter put controller side.



APU\_CORE  
TDC 35A(1H1L)  
Peak current 45A  
OCP current > 55A

FSW=400kHz  
DCR 1.19mohm +/-5%

H/S Rds(on) 6.8mohm , 8.6mohm  
L/S Rds(on) 2.0mohm , 2.5mohm

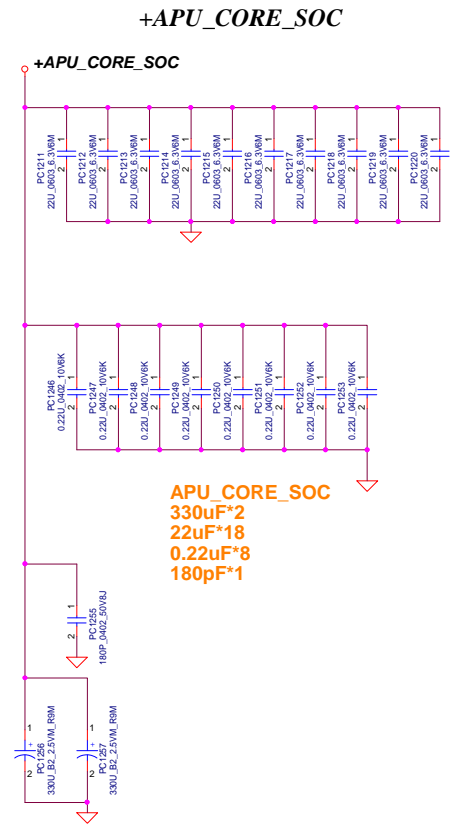
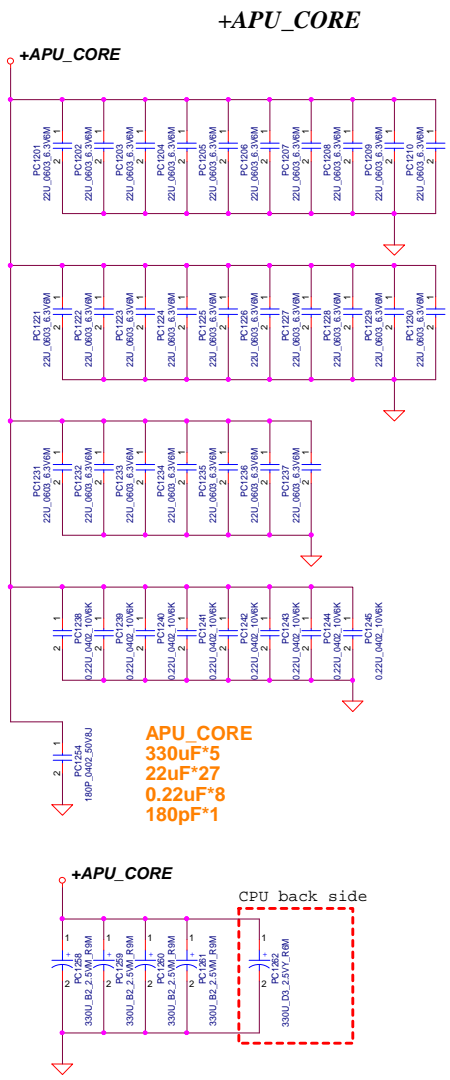
APU\_CORE\_NB  
TDC 19A(1H1L)  
Peak current 13A  
OCP current > 16A

FSW=400kHz  
DCR 1.19mohm +/-5%

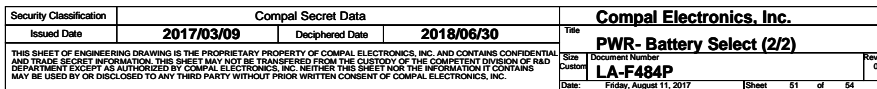
H/S Rds(on) 6.8mohm , 8.6mohm  
L/S Rds(on) 2.0mohm , 2.5mohm

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				Date	2017/08/11/2017









Item	Reason for change	PG#	Modify List	Date	Phase
1	Consider component de-rating		Change PF3 from SP040003U00(S FUSE 0438005.WR 5A 32V UL/CSA FAST) to SP040003Q00(S FUSE S1206-H-7.0A 7A 32V UL FAST)	6/23	EVT
2	To avoid acoustic issue		Change PC906,PC1004,PC1005,PC1017,PC1018,PC1037,PC1038,PC804,PC805 ,PC816,PC817 from SE000000QK00(S CER CAP 10U 25V K X5R 0805 H1.25) to SE000000X200(S CER CAP 10U 25V M X5R 0603)	6/23	EVT
3	Change 5VLD0_EN to reserve		Add PR464(SD013000080,S RES 1/10W 0 +-5% 0603) Delete PQ455(SB000000VY00,S TR LSK3541G1ET2L 1N ) Delete PQ452(SB934130000,S TR AO3413 1P SOT-23 ) Delete PR462,PR463,PC463	6/23	EVT
4	To reduce VS LDO component		Delete PQ1601(SB000000VY00,S TR LSK3541G1ET2L 1N ) Delete PD1603(SCS00001200,S SCH DIO BAS40CW SOT-323 ) Delete PR1601,PR1602	6/23	EVT
5	Add remote sensing to +0.8VALW		Add PQ601(SB000000VY00,S TR LSK3541G1ET2L 1N ) Add PR618	6/23	EVT
6	Modify 2nd battery circuit		Change PD1601 from SC1N4148180(S DIO 1N4148WS-7-F SOD-323) to SCS000000Z00(S SCH DIO RB751V-40 SOD-323) Add PD1603(SCS000000Z00,S SCH DIO RB751V-40 SOD-323)	6/23	EVT
7	Modify APU_CORE & APU_CORE_SOC switching frequency from 300K to 400K		Change PR1015 & PR1016 to 0_0402_5% Change PR1018 to 69.8K_0402_1% Change PR1019 to 32.4K_0402_1%	6/23	EVT
8	Modify +0.8VALW OCP setting(min 9.5A)		Change PR612 to reserve	6/23	EVT
9	Modify BATGONE circuit		Change PR130 to 10K_0402_1% Add PC134 to 0.47U_0402_6.3V6K	6/23	EVT
10	Modify BATGONE circuit		Add PR135(0_0402_5%)	6/29	EVT
11	Modify +0.95VGS output voltage		Change PR1502 from 20K_0402_1% to 10K_0402_1%	6/29	EVT
12	Reduce S5 leakage current		Change PR413 from 47.5K to 475K Change PR414 from 10K to 100K	6/29	EVT
13	Remove PD function		Delete PC5,PC6,PC9,PD1,PQ1,PQ2,,PR1,PR2,PR3,PR5,PR6,PR7,PC12,PC13, PC14,PC15,PD3,PF3,PQ3,PQ4,PR16,PR17,PR18,PR19	6/29	EVT
14	Change charger IC solution to ISL88739A			6/29	EVT
15	Modify power sequence for GPU		Change PR902 from 0_0402_5% to 88.7K_0402_1% Change PR1503 from 0_0402_5% to 47K_0402_1% Add PC902 & PC1504(0.1U_0402_10V7K)	7/5	EVT
16	Change GPU CORE solution for R17M-P1-50 GPU		Change PU801 from RT3662EB to RT3662AC	7/25	EVT
17	Delete +0.95VGS power rail for GPU change		Delete PU1501	7/25	EVT
18	Change DDR power solution for cost saving		Change PU501 from SY8210AQVC to RT8207P	7/25	EVT
19	For reduce S5 leakage current , turn off selector in S5		Add PQ1662 ,PQ1663 Add PR1684 , PR1683 , PR1682, PR1691 , PR1685 Add PC1660 , PC1664	7/25	EVT
20	Add proshot function when 2nd battery removed		Add PQ1667 . PR1689 , PR1690 , PC1663	7/25	EVT
21	Modify 2nd battery circuit		Add PQ1666 , PQ1664 , PQ1665 , PD1653 Add PR1666 , PR1687 , PR1692	7/25	EVT
22	Modify for power sequence		Add PR613(100K_0402_5%)	8/8	EVT
23	Modify VGA CORE CHOKE and OCP setting		Change PL801,PL802 from 0.15UH +-20% 36A 7X7X4(SH00001EE00) to 0.15UH +-20% 35A 7X7X3(SH00001EF00) Change PR807,PR832 from 1.1K_0603_1% to 909_0603_1% Change PR816,PR843 from 1.1K_0402_1% to 909_0402_1% Change PR847 from 13K_0402_1% to 11.5K_0402_1% Change PR848 from 13.7K_0402_1% to 15K_0402_1% Change PR849 from 5K_0402_1% to 2.8K_0402_1%	8/9	EVT

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HW SIV PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	17/02/13	25,34	Connect 5VLDO_EN (EC GPIO57) to control 5V power IC	Reserve EC recovery solution for S5 shutdown can't boot when Type-C device insert into Type-A connector.
2	17/2/13	8	Change Touchpad I2C port from I2C3 to I2C0	Follow AMD suggestion
3	17/02/15	30	Change +0.95VALW to +0.95VS solution from dual load power switch to single N-MOSFET	For AMD APU load transient test result
4	17/02/15	30	Change +1.8VALW to +1.8VS solution from dual load power switch to single N-MOSFET	To save layout space due to 0.95v solution change
5	17/02/18	27	Connect UT1.A1 (NXP high voltage protection IC) to +USBC_VBUS	Follow Type-C EA test result
6	17/02/20	8	Swap DGPU_PWROK(APU AGPIO90) for TP_INT# (APU AGPIO85)	Follow AMD suggestion